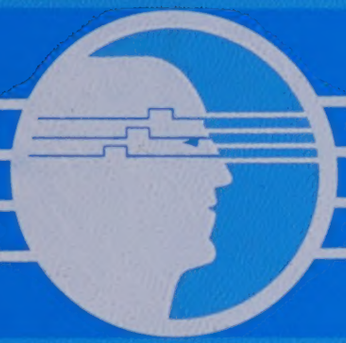

THE LEADER IN..
TECHNOLOGY
PERFORMANCE
AND INNOVATION

GOULD Electronics

Gould Inc.

Design & Test Systems Division

Publication Number 0120-0054-10
November 1984

K205 LOGIC ANALYZER

SERVICE MANUAL

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11/84

K205 Logic Analyzer

WARNING

This equipment has not been tested to show compliance with new FCC Rules (47 CFR Part 15) designed to limit interference to radio and TV reception. Operation of this equipment in a residential area is likely to cause unacceptable interference to radio communication requiring the operator to take whatever steps are necessary to correct the interference.

The following procedures may help to alleviate the Radio or Television Interference Problems:

1. Reorient the antenna of the receiver receiving the interference.

2. Relocate the equipment causing the interference with respect to the receiver (move or change relative position).

3. Reconnect the equipment causing the interference into a different outlet so the receiver and the equipment are connected to different branch circuits.

4. Remove the equipment from the power source.

NOTE:

The user may find the following booklet prepared by the FCC helpful: "How to Identify and Resolve Radio-TV Interference Problems". This booklet is available from the U.S. Printing Office, Washington, D.C. 20402. Stock No. 004-000-00345-4.

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PREFACE

This manual contains information for servicing and maintaining the Gould K205 Logic Analyzer. Procedures are provided for making adjustments and calibrating the control circuits for various functions. These procedures include the use of diagnostic tests to troubleshoot and isolate a malfunction to a circuit component. Theory of operation is presented for the printed circuit board functions. Service aids in the form of schematic diagrams, wiring diagrams, assembly drawings, cable connection diagrams and parts lists are included for user reference.

The material in this manual reflects the Control Firmware level valid on October 1, 1984, and is up-to-date at the time of publication, but is subject to change without notice.

Copies of this publication and other Gould Inc., Design and Test Systems Division Publications may be obtained from the Gould Inc., Design and Test Systems Division sales office or distributor serving your locality.

RELATED PUBLICATIONS

The following support documentation may be used in conjunction with this manual:

> K205 User's Manual, Publication Number 0120-0014-10 which describes the capabilities, functions, and operation of the K205 Logic Analyzer.

ASSISTANCE

If you require assistance on this product, please call Gould Inc., Design and Test Systems Division Customer Service on the toll-free, hot-line number listed below.

Nationwide (800) 538-9320/9321

California (800) 662-9231

WARRANTY

The Gould Inc., Design and Test Systems Division K205 is warranted against defects in materials and workmanship for a period of one year from date of shipment. Any floppy disk or hard disk drives attached to or contained within this equipment are warranted for 90 days from date of shipment. Gould Inc., Design and Test Systems Division will repair or replace products that prove to be defective during the warranty period.

Warranty service must be performed at a Gould Inc., Design and Test Systems Division authorized service facility. **The customer must call Gould's Customer Service department at the toll-free numbers listed in the front of this manual and obtain a Return Authorization number prior to returning the unit for service.** If a unit fails within 30 days of shipment date, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the 30-day period, should be sent to Gould Inc. prepaid, and Gould Inc. will return the unit prepaid. The customer must pay all shipping charges for units out of warranty.

Misuse of, abuse of, or tampering with this unit will, at the discretion of Gould Incorporated, cause this warranty to be null and void.

CONTENTS

Chapter — Page

1 GENERAL DESCRIPTION
- INTRODUCTION....1-1
  - Overview of K205 Features....1-1
  - Overview of Manual Contents....1-3
- SERVICING PHILOSOPY....1-4
  - Power Up Diagnostic Routines....1-4
  - DOS Diagnostic Routines....1-5
- MAINTENANCE FEATURES....1-5
  - Probe Test....1-6
  - Display Calibration Pattern....1-6
- SPECIFICATIONS....1-6
  - K205 Unit Configurations....1-6
  - Power Requirements....1-7
  - Physical Dimensions and Weight....1-7
  - Environmental Limits....1-7
  - Probes....1-7
  - Data Inputs....1-8
  - Clocks....1-8
  - External Clock Specifications....1-9
  - Data Set Up and Hold Time....1-9
  - DVM Inputs....1-9
  - Signal Outputs....1-10
  - Memory....1-10
  - Trace Control....1-10
  - Interface....1-10
  - Audible Tone Signal....1-10

2 SYSTEM COMPONENTS AND INTERCONNECTIONS
- INTRODUCTION....2-1
- BOARDS AND COMPONENTS....2-1
- BOARD AND COMPONENT INTERCONNECTIONS....2-4
  - Boards....2-4
  - Components....2-4
- CARD CAGE ARRANGEMENT....2-6
  - Data Board Configurations....2-6
  - Board Calibration Controls....2-7
- SUGGESTED TEST EQUIPMENT....2-7

3 CALIBRATION AND POWER UP DIAGNOSTICS
- GENERAL....3-1
- POWER UP DIAGNOSTICS....3-1
  - Diagnostic Operation....3-1
  - User Interaction....3-2
  - Microprocessor RAM Test Description....3-2
  - Microprocessor ROM Checksum Test Description.3-3
  - Keyboard Stuck Key Test Description....3-3
  - Voltage Test Description....3-4
  - Display Board CMOS RAM Test Description....3-4

Chapter Page

3 CALIBRATION AND POWER UP DIAGNOSTICS (Cont'd.)
PROBE TEST....3-5
Probe Test Pattern Generator....3-5
Probe Connections....3-5
Default Setup....3-5
Fixed ECL Threshold Setup....3-6
Record/Review Test Results....3-6
DISPLAY CALIBRATION....3-8
Calibration Requirements....3-8
Display Adjustment Points....3-8
POWER SUPPLY VOLTAGE MEASUREMENTS....3-11
REFERENCE/THRESHOLD VOLTAGE AND DVM CALIBRATION....3-13
10V Reference Voltage Adjustment....3-13
TTL Threshold Adjustment....3-14
ECL Threshold Adjustment....3-16
Variable A Threshold Adjustment....3-17
Variable B Threshold Adjustment....3-18
DVM Adjustment....3-19
INTERNAL CLOCK ADJUSTMENT....3-20

4 THEORY OF OPERATION
GENERAL....4-1
OVERVIEW OF K205 UNIT OPERATION....4-1
MPU Board Interaction....4-1
Data Board Interaction....4-3
Clock Board Interaction....4-3
Control Board Interaction....4-3
Threshold/GPIB/RS-232 Board Intreaction....4-3
Data Display Board Interaction....4-4
DATA DISPLAY BOARD OPERATIONS....4-5
Overview....4-5
CRT Controller....4-5
Interrupt Processor....4-8
Keyboard and Front Panel Interface Circuit....4-8
CMOS RAM Save Circuit....4-8
Real Time Clock....4-9
Audio Error Alarm Circuit....4-9
DOS Interface Circuit....4-9
MPU BOARD OPERATIONS....4-10
Overview....4-10
Microprocessor....4-10
Address Registers and Data Transceivers....4-12
Memory....4-12
Memory Controller....4-12
I/O Decoding....4-13
THRESHOLD/GPIB/RS-232 BOARD OPERATIONS....4-14
Overview....4-14
Threshold Circuit....4-14
DVM Circuit....4-16
GPIB Interface Circuit....4-16
RS-232 Interface Circuit....4-16
MPU Interface....4-16

Chapter Page

4 THEORY OF OPERATION (Cont'd.)
CLOCK BOARD OPERATIONS....4-18
Overview....4-18
Internal Clocks....4-18
External Clocks....4-20
AND Master Clocks....4-20
OR Clock Selection....4-21
Level Memory Circuit....4-21
MPU Interface....4-21
DATA BOARD OPERATIONS....4-23
Overview....4-23
Data Input Control....4-23
Operating Modes....4-25
Sampling Circuit....4-25
Data Pipeline Control....4-25
Memory Control....4-26
MPU Interface....4-26
CONTROL BOARD OPERATIONS....4-26
Overview....4-27
Word Recognition Circuits....4-27
Word Selection Circuits....4-29
Level Switching Circuits....4-30
Delay Counter....4-30
Recording Control Circuits....4-30
MPU Interface....4-32

5 DISK DIAGNOSTICS
INTRODUCTION....5-1
STARTING UP THE K205 DIAGNOSTICS....5-3
DIAG MENUS AND DISPLAYS....5-3
Main Menus....5-3
System Testing (All Active Boards)....5-4
Single Board Testing....5-5
Conducting all Subtests or Individual Tests..5-5
DIAGNOSTIC PARAMETERS (EDIT KEY)....5-5
General....5-5
Halt on Error....5-6
Loop on Error....5-6
Display Error Messages....5-7
Number of Times to Repeat Test(s)....5-7
Test Drive A, Test Drive B....5-8
Test Side 0, Test Side 1....5-8
Run Operator Action Tests....5-8
PASS/ERROR TABULATION (DATA KEY)....5-9
DIAGNOSTIC RE-INITIALIZATION AND EXIT TO SYSTEM...5-10
General....5-10
Exiting the Diagnostic....5-10
SUMMARY OF DIAGNOSTIC OPERATING SYSTEM KEYS....5-11
KEYBOARD/DISPLAY BOARD DIAGNOSTIC TEST....5-12
DATA BOARD DIAGNOSTIC TEST....5-23
CONTROL BOARD DIAGNOSTIC TEST....5-51
CLOCK BOARD DIAGNOSTIC TEST....5-74
THRESHOLD/GPIB/RS-232 BOARD DIAGNOSTIC TEST....5-115
STORAGE CONTROLLER BOARD DIAGNOSTIC TEST....5-136

Chapter Page

6 SCHEMATICS AND DRAWINGS
GENERAL....6-1
LIST OF DRAWINGS....6-1

Figure Page

1-1 K205 Logic Analyzer, General Arrangement....1-2
2-1 K205 Front Panel Arrangement....2-3
2-2 K205 Rear Panel Arrangement....2-3
2-3 K205 System Interface of Components to Mother Board....2-5
2-4 K205 Card Cage Arrangement....2-6
3-1 Typical Probe Test Recording Using ECL Threshold....3-7
3-2 CRT Centering Rings....3-9
3-3 Data Display Board Adjustment Points....3-10
3-4 CRT Grid Pattern....3-10
3-5 Power Supply Voltage Measurements....3-12
3-6 Threshold/GPIB/RS-232 Board Adjustments....3-14
3-7 Test Connections for Threshold Voltage Adjustment....3-15
3-8 Clock Board, Internal Clock Adjustment....3-21
4-1 K205 System Data Flow and Control Block Diagram....4-2
4-2 Data Display Board, Block Diagram....4-6
4-3 MPU Board, Block Diagram....4-11
4-4 Threshold/GPIB/RS-232 Board, Block Diagram....4-15
4-5 Clock Board Block Diagram....4-19
4-6 Data Board, Block Diagram....4-24
4-7 Control Board, Block Diagram....4-28
5-1 Organization of K205 Diagnostic Software....5-2

Chapter 1

GENERAL DESCRIPTION

INTRODUCTION

Overview of K205 Features

The Gould Model K205 Logic Analyzer (Figure 1-1) is a precision test instrument that monitors and records logic signals generated by the user's high speed digital logic based equipment. The K205 accepts 32 standard (or 48 extended) data inputs and 8 standard (or 12 extended) external clock inputs supplied via probe interface circuits.

The K205 internal control logic performs measurements on the input signals to accomplish comparison analysis, capture of data samples, correlation of data characteristics, and recording the results in memory. The measurement operations are menu-driven by resident firmware which is controlled by manipulating various function keys located on the front panel. The menu displays allow the user to set up test conditions, capture the analysis results for binary logic states associated with data-domain analysis, and collect pulse-train waveforms associated with time-domain analysis.

The menu-driven displays provide fast, convenient access to all logic analyzer capabilities and allow the user to define parameters for threshold logic levels and timing relationships of sample inputs. Major features of the K205 operation are summarized in the following list:

- The K205 equipment functions are menu-driven under the control of a 16-bit, 8086 microprocessor.
- The operating system accommodates up to 256K bytes of RAM and 128K bytes of ROM.
- Three input sections, A, B, and optional C, accept user inputs via probe circuits. Each section is subdivided into two input groups. Each input group accepts 8 data and 2 clock signals to provide a total of 48 data inputs and 12 external clocks.
- Data inputs are capable of being sampled internally at frequency rates up to 100 MHz. Data may be displayed in 40-column Binary format or in Hexadecimal, Octal, ASCII, EBCDIC, or user defined format.
- Three different input modes, Sample, Glitch, and Latch/Demultiplex can be selected in groups of 8 or 16 channels.
- Independent threshold-level selection is provided for each logic probe and associated group of clocks.
- Up to 16 different state levels for trace control are selected by using the display menus and front panel keys.

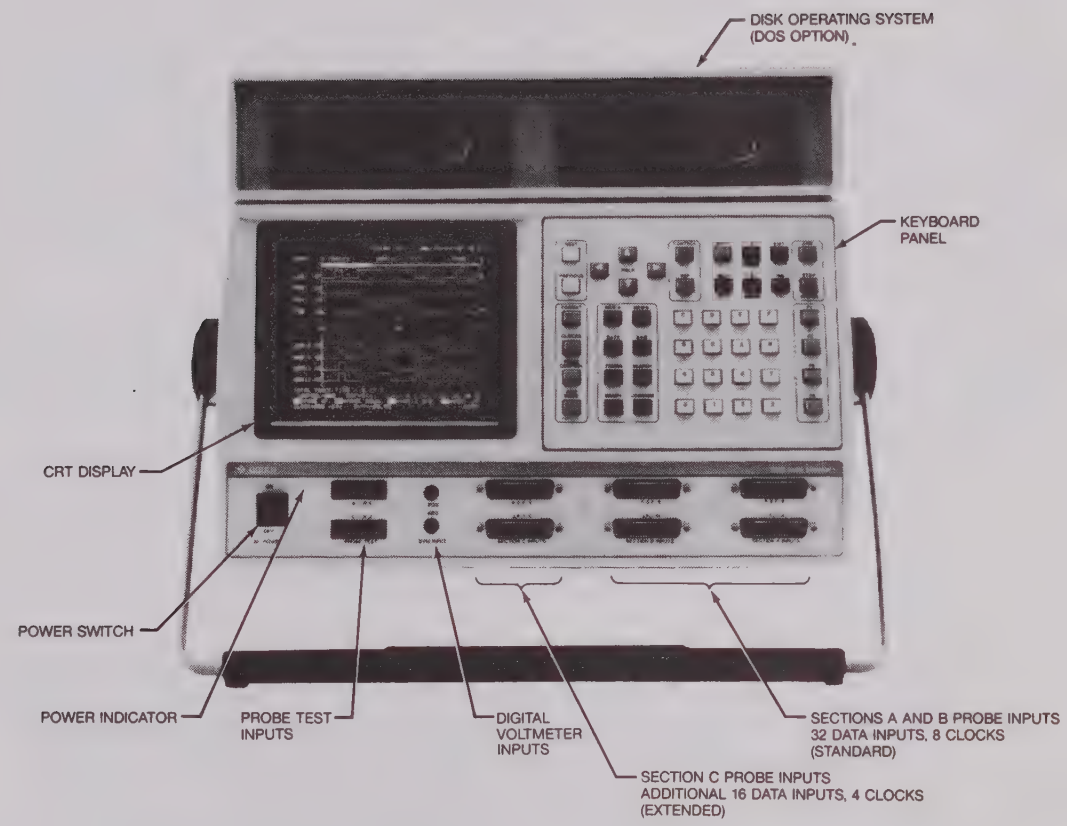


Figure 1-1 K205-D Logic Analyzer, General Arrangement

- The K205 can correctly track a 50MHz state machine, simultaneously comparing the machine state to four search patterns per level every 20 nanoseconds.
- The trace is recorded in a 48-bit wide x 515-word length memory.
- A 24-hour Real-Time clock with battery backup feature allows the K205 to log the current time of day and date of each recording.
- The battery backup feature also drives the CMOS memory which preserves the current set up for recording parameters if power is interrupted.
- A built-in Digital Voltmeter (DVM) with input jacks on the front panel provides a 4-digit readout for user convenience.
- A self-contained frequency counter provides automatic measurement of external clock frequency and status.
- The K205 may be operated as a stand-alone unit or interfaced with the user's external CPU system or peripherals via an RS-232-C or IEEE-488 communications link.
- An optional Disk Operating System (DOS) provides a capability for storing set up information and data on a floppy disk for later restoration. The DOS option also provides a capability for loading and executing disk-based diagnostic routines.

Overview of Manual Contents

The organization and scope of this manual describes the K205 circuit characteristics and component functions as applicable for servicing and calibrating the unit to maintain its accuracy and availability for use. Service aids in the form of schematic/wiring diagrams, assembly drawings, cable connection diagrams, and parts lists are included for reference purposes. The manual content is arranged as follows:

Chapter 1. GENERAL INFORMATION - This chapter presents an overview of the K205 operating features, organization of manual contents, servicing philosophy, maintenance features, and equipment specifications.

Chapter 2. SYSTEM COMPONENTS AND INTERCONNECTION - This chapter describes the interconnection of printed circuit boards, power distribution, external I/O interface, and special tools and test equipment.

Chapter 3. CALIBRATION AND POWER UP DIAGNOSTICS - This chapter describes the power up Boot PROM check, Probe Test, calibration of the Data Display Board, Clock Board, and Threshold/GPIB/RS-232 Board, and measurement of the power supply voltages.

Chapter 4. THEORY OF OPERATION - This chapter presents theory of operation for each printed circuit board and associated circuitry.

Chapter 5. DOS DIAGNOSTICS - This chapter presents a description of each diagnostic module and its associated subtests. Procedures are included for loading the diagnostic program from the disk, selecting the diagnostic test, setup of test parameters, executing the test routines, and interpreting the results.

Chapter 6. SCHEMATIC DIAGRAMS AND PARTS LISTS - This chapter provides reference material such as schematic diagrams, assembly drawings, and parts lists.

SERVICING PHILOSOPHY

Maintenance strategy for the K205 involves the use of diagnostic routines to isolate a defective circuit function for repair or replacement of boards at the user's site. The K205 contains firmware diagnostic routines that perform an operational check of major circuit functions whenever the unit is reset or powered up from a cold start. Malfunctions detected by the firmware diagnostics may be tested further by using the Disk Operating System (DOS) diagnostic routines to isolate the cause of failure. The resident firmware also generates special displays which permit the user to conduct input Probe Tests and perform CRT alignment.

The use of any diagnostic for troubleshooting does not eliminate the need for user interaction to visually inspect cable connections, ensure printed circuit boards are seated properly, and ensure calibration adjustments are made within prescribed limits. The diagnostic should be rerun after a repair is completed to verify the problem is resolved before the unit is placed into operation.

Power Up Diagnostic Routines

The Power Up Diagnostic routines provide a general indication of the system operational status. Appropriate messages are displayed on the CRT to identify the type of error condition and the failed function. Since several interacting components may be associated with the resulting malfunction, basic board-swapping techniques and rerunning the diagnostic may be employed to accomplish the repair. To avoid possible damage to equipment, do not remove or install a printed circuit board while AC or DC power is applied to the unit. The following circuit functions are tested by the Power Up Diagnostic routines:

- MPU Board RAM test
- MPU Board ROM test
- Keyboard Matrix test for stuck keys
- System voltage tolerance test
- Display Board CMOS RAM Test
- Threshold/GPIB/RS-232 Board Check

Power UP Diagnostic Routines (cont'd)

- DOS Recognition Check
- Data Board Recognition Check
- Clock Board Recognition Check
- Control Board Recognition Check

DOS Diagnostic Routines

The K205 Disk Operating System (DOS) option provides a capability for loading diagnostic routines from the disk to further isolate the cause of failure to a specific circuit or component. The DOS loader firmware, however, must be functional to effect loading of the diagnostic software from the disk. The DOS diagnostic provides flexibility for the user to set up test parameters that halt on error, loop on error, perform repetitive tests for a specified pass count, etc. The DOS diagnostic is fully described in Chapter 5.

A separate diagnostic routine is provided for each component. The diagnostic does not assume any part of the system is functional until it has passed its associated subtests. If a failure is detected, the diagnostic monitor generates an error message identifying the cause of failure. A Self Test menu is displayed when the DOS diagnostic is invoked. The following software is contained on the diagnostic disk:

- Diagnostic Operating System (K205)
- Keyboard/Display Diagnostic Module (KDDIAG)
- Threshold/GPIB/RS-232 Diagnostic Module (THDIAG)
- Control Board Diagnostic Module (CBDIAG)
- Clock Board Diagnostic Module (CKDIAG)
- Data Board Diagnostic Module (DBDIAG)
- Storage System Controller Diagnostic Module (SCDIAG)

When the user selects a test for execution, the diagnostic test monitor generates detailed sub-menus that direct the user in running the test procedure.

MAINTENANCE FEATURES

In addition to the power up diagnostics firmware, the K205 contains additional built-in features that aid in maintaining the equipment. These features, also driven by resident firmware, allow the user to test the sample and clock inputs at each probe and to align the CRT display characteristics. An overview of these features is presented in paragraphs that follow.

Probe Test

Two Probe Test connectors, located on the front panel, allow the user to verify that two clock inputs and eight data inputs supplied from each probe, operate within acceptable limits. A test pattern generated by the K205 firmware is supplied to the probe under test. Procedures for conducting the Probe Test are described in Chapter 3.

Display Calibration Pattern

Procedures for calibrating the CRT are described in Chapter 3. The Display Calibration Pattern, is accessed by depressing and holding the SHIFT key while powering up the unit. This pattern allows the user to make adjustments on the Display printed circuit board for calibrating the following display characteristics:

- Vertical Height
- Vertical Hold
- Horizontal Width
- Horizontal Linearity
- Vertical Linearity
- Focus
- Brightness

SPECIFICATIONS

The following is a summary of the physical, environmental, and operating characteristics of the K205.

K205 Unit Configurations

Standard Unit:	Provides inputs for 32 data signals and 8 clocks via input Sections A and B.
Extended Unit:	Provides inputs for 48 data signals and 12 clocks via input Sections A, B, and C.
Section C Option:	Provides probe inputs for 16 add-on data signals and 4 additional clocks via input Section C.
DOS Option:	Disk Operating System provides two 5 1/4" floppy disk drives mounted in an add-on assembly unit which provides 312K bytes of storage per disk.

Power Requirements

Input Frequency: 50 or 60 Hz
Input Voltage: 90 to 135 VAC or 180 to 270 VAC
Input Power: 500 Watts without DOS option or 550 Watts with DOS option

Fuses for Rated Voltage:	Voltage Range	Fuse
	90 VAC to 135 VAC	3AG, 8 Amp
	180 VAC to 270 VAC	3AG, 4 Amp

Physical Dimensions and Weight

Height: 8.6 inches (21.8 Cm) without DOS, 12 inches (30.1 Cm) with DOS
Width: 17.5 inches (44.5 Cm)
Depth: 24.7 inches (62.7 Cm) including handle

Weight: 45 lbs. (20 Kg) without probes or DOS

55 lbs. (25 Kg) without probes

Environmental Limits

Ambient Temperatures: 39 to 115 Deg.F (4 to 46 Deg.C) OPERATING
-8 to 117 Deg.F (-20 to 50 Deg.C) STORAGE

Relative Humidity: 20% to 80% OPERATING
1% to 95% STORAGE

Max Wet Bulb: 78 Deg.F (25 Deg.C) OPERATING
No condensation STORAGE

Probes

Loading Characteristics:

Signal Inputs

Input resistance: 1 megohm referenced to threshold
Input capacitance: < = 6pF (< = 15 pF with flying leads)

NOTE: Input resistance may approach 500K ohms at voltages exceeding +/- 15 volts from threshold.

Maximum input without damage: +/- 50 volts peak

Common mode range: +/- 0.5 volt maximum between probe and unit probed

Ground Input: Input resistance is 91K ohms referenced to chassis

Probe Transfer Characteristics:

Bandwidth to 90% volts out: = >100 MHz

Minimum swing for output: Threshold +/- 0.20 V maximum

Threshold variance: +/- 15 Mv maximum, between input signals;

+/- 30 Mv maximum, any two probes

Input compensation: Even to 20% overcompensated

Thresholds: Thresholds are independently selectable for each probe and the clocks as follows:

TTL, +1.4 volts

ECL, -1.3 volts

VAR A and VAR B

NOTE: Variable thresholds may be set from -9.99 volts to +9.99 volts in 0.01 volt increments. Accuracy of all threshold voltages is 30Mv.

Polarity: + or - is selectable for each signal

Data Inputs

32 standard (or 48 extended) data inputs configured in two (or three) input sections, A, B and C. Each section contains two input groups that accept 16 signals (one group for lower Bits 7-0, the other group for upper Bits F-8).

Input Modes: Sample Mode
Latch and Demultiplex Mode
Glitch Mode

Input Frequency: DC to 100 MHz (data)
DC to 50 MHz (clocks)

Clocks

The 32-standard input configuration provides 6 Sample (edge-sensitive) clocks and 2 Latch Enable (level-sensitive) clocks for a total of 8 external clocks.

The 48-extended input configuration provides 6 Sample (edge-sensitive) clocks and 6 Latch Enable (level-sensitive) clocks for a total of 12 external clocks.

Internal: Internal clock is selectable from 20 ns (50 MHz) to 100 ms (10Hz) in decades of time which is divided by units of 1 to 10 (i.e., 100ns, 1 us, 10 us and 1 us, 2 us, 3 us,... 10 us). One internal clock may be programmed per recording.

A 10 ns (100 MHz) clock is available to the Sample/Store sections in addition to the internal or external clock.

External: Twelve external clock inputs which may be combined to form three Sample clocks, three Latch Enable clocks, and one Master (M) clock.

Sample clock: One sample clock may be specified for each input section (A, B, or C) to hold data for the master clock, or move trace data into memory (effective for internal, external, and 100 MHz clocks). This clock is edge sensitive.

Latch clock: A special case of Sample Mode which is used to temporarily hold (by latch) the first byte of multiplexed data. When the latch clock goes false, data is held in the input latched (until the latch clock returns to true). The master clock or sample/store clock then moves the latched sample (or the present data, if latch is true) into the pipeline (effective for external clocks only). This clock is level sensitive.

M-CLock: The master clock is used to shift samples into memory and the trace control logic (effective for internal or external clocks). This clock is edge sensitive.

External Clock Specification:

Frequency: DC to 50 MHz

Pulse Width: 8 ns Minimum

Clock Skew: 7 ns Maximum between any two clock combinations

Latch Clocks Setup: 13 ns Minimum before Sample Clocks

Clock Frequency Measurement: The K205 automatically measures the external clock frequency from 100 Hz to 50 MHz with 0.1% accuracy

Data Set Up and Hold Time

Data must be present 12 ns maximum before, and stable until, the clock active edge. Typical setup time is 8 ns.

Data may change zero ns after the clock active edge

Minimum detectable pulse width is one clock period +5 ns

DVM Input

Range: +/- 20 VDC Maximum

Resolution: 20 mv

Input Impedance: 20k ohms

Accuracy: +/- 0.5%

Signal Outputs

VIDEO, BNC connector: 1 Vp-p into 75 ohms composite video output is compatible with RS-170

CLOCK, BNC connector: ECL active low corresponds to the internal clock

GET, BNC connector: Group execute trigger pulse output for the IEEE-488 Command - TTL

TRACE BNC connector: TTL high output when trace is enabled

Two LEMO power output connectors: +5V and -5.2V @ 300 mA

Memory

The K205 contains main memory M, storage memory A, and reference memory B. Memory M is organized as 515 by 36 or 52 bits. Four bits of each word are used to store the level at which data was recorded. The CPU reads data from M into A or from A into B. Both A and B are a part of the CPU memory.

The operating system accommodates up to 256k bytes of RAM and 128k bytes of ROM under the control of the 16-bit, 8086 CPU.

Trace Control

Trace control employs 16 trace levels that are defined by user inputs via the display menu and keyboard. Four commands are decoded for each of the sixteen levels. The four commands are TRACE, STOP, JUMP, and ADVANCE. Control begins at level zero and automatically stops on advance from level F.

A delay counter may be programmed from 1 to 65,535 clocks or events to begin tracing after the specified condition occurs. The rear panel BNC output for TRACE is at a TTL level that goes high while the K205 is tracing.

Interface

One RS-232-C Serial I/O Port configured as Data Terminal Equipment (DTE) six-wire system

One Auxiliary Serial I/O Port for RS-232-C (reserved for K205 options)

One IEEE-488 Bus Interface, Parallel Port with Talker/Listener configuration selectable by the user via software control

Timer: A 24-hour, time-of-day clock is backed up by a 2.9 V battery

Back Up Memory: A 2k x 16 CMOS memory with battery backup saves the setup of recording parameters if power is interrupted or when the unit is turned off.

Audible Tone Signal

An audible tone signal (beeper) which indicates keystroke errors can be enabled or disabled by the user via a menu display.

SYSTEM COMPONENTS AND INTERCONNECTIONS

INTRODUCTION

This chapter describes individual printed circuit boards and components that comprise the K205 Logic Analyzer. Further descriptions are included for the interconnection of these boards and components along with the equipment that is necessary for making repairs. Front and rear views of the K205 chassis are shown in Figures 2-1 and 2-2.

BOARDS AND COMPONENTS

The following boards and components are used for K205 hardware configurations:

- Keyboard--The keyboard, configured as a scanned matrix, consists of 48 keys, many of which can be shifted to perform a second function. Because of the shift capability, 20 keys can perform as a full alpha-numeric keyboard.

- Front Connector Panel--The front connector panel contains the following components:

  - Six DB-25 female connectors for external data/clock input
  - Two jacks for DVM (POS and NEG) input
  - Two card-edge female connectors for PROBE TEST output
  - Power LED indicator
  - AC power switch

  - The data/clock input connectors that are available for the standard (32) or extended (48) input configuration is established by the number of Data Boards installed. The unit may be configured with two or three Data Boards which accommodate 32 or 48 inputs respectively. The Configuration Display screen indicates the number of active connectors present for a given instrument.

  - Illumination of the Power LED indicator also indicates the presence of -5 VDC when AC power is applied.

- Display Assembly--The display assembly consists of an 8-inch, P39 CRT and a CRT deflection yoke with cable harness. The mounting bracket for the assembly is an integral part of the CRT glass envelope.

- Rear Connector Panel--The rear connector panel provides external interface for signal I/O and power via the following circuit components:

  - Signal output is provided for VIDEO, CLOCK, TRACE, and GET via four BNC connectors.

- Rear Connector Panel (Cont'd)

  - The + 5V and - 5V output is provided by each of two LEMO connectors

  - Signal I/O is provided by one IEEE-488 connector and two RS-232 connectors (one of which is labeled AUX and is intended for future options).

  - Power Interface is provided by the 120/240 VAC line voltage input socket, the line voltage select switch (for 120/240 VAC), and the power fuse rated at 8 Amp, 3AG for 120 VAC or 4 Amp, 3AG for 240 VAC power input.

- Power Supply--The power supply is a switching type supply which provides the following outputs:

  + 5VDC at 11 Amps

  - 5.2VDC at 36 Amps

  +15VDC at 3.0 Amps

  -15VDC at 0.2 Amp

  -2VDC at 17 Amps

- Data Board--The Data Board Assembly interfaces the ECL devices of the probes to the TTL devices of the board. The Data Board processes 16 inputs. Either two or three Data Boards will be installed in a given system configuration as determined by the 32 or 48 input capability.

  - The Data Board main memory is 515 bits deep by 48 bits wide and gathers data at 100MHz.

- MPU Board--The MPU Board Assembly contains the 8086 microprocessor and operates as the controller for K205 operations. The operating firmware resides in ROM located on the MPU Board.

- Control Board--The Control Board Assembly provides the user with a menu driven display that allows 16 trace levels to be programmed by the user. A selection of qualifiers enables the user to pick and choose the information that will be recorded. The Control Board also provides an output signal to the rear panel TRACE BNC connector.

- Threshold/GPIB/RS-232 Board--The Threshold/GPIB/RS-232 Board Assembly provides fixed and variable threshold voltages for the probe pods. In addition, this board provides two RS-232 ports(one of which is intended for future options) and one IEEE-488 Talker/Listener port. This board also contains control circuits for DVM input and provides an output signal to the rear panel GET BNC connector.

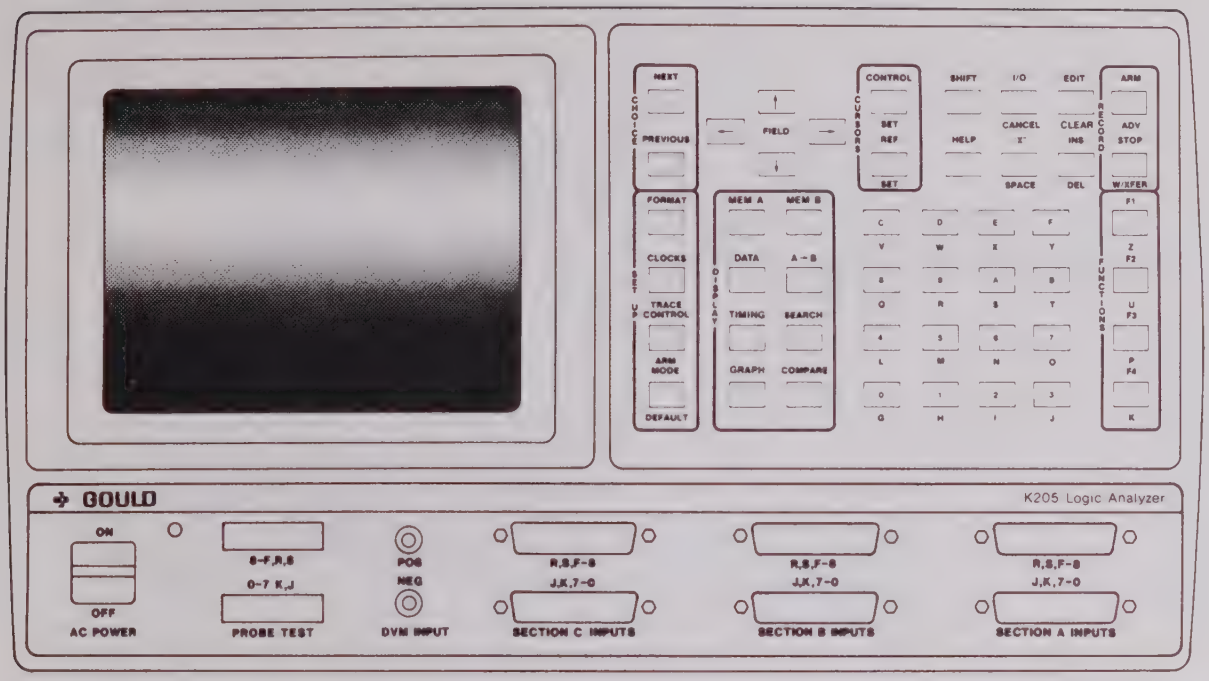


Figure 2-1. K205 Front Panel Arrangement

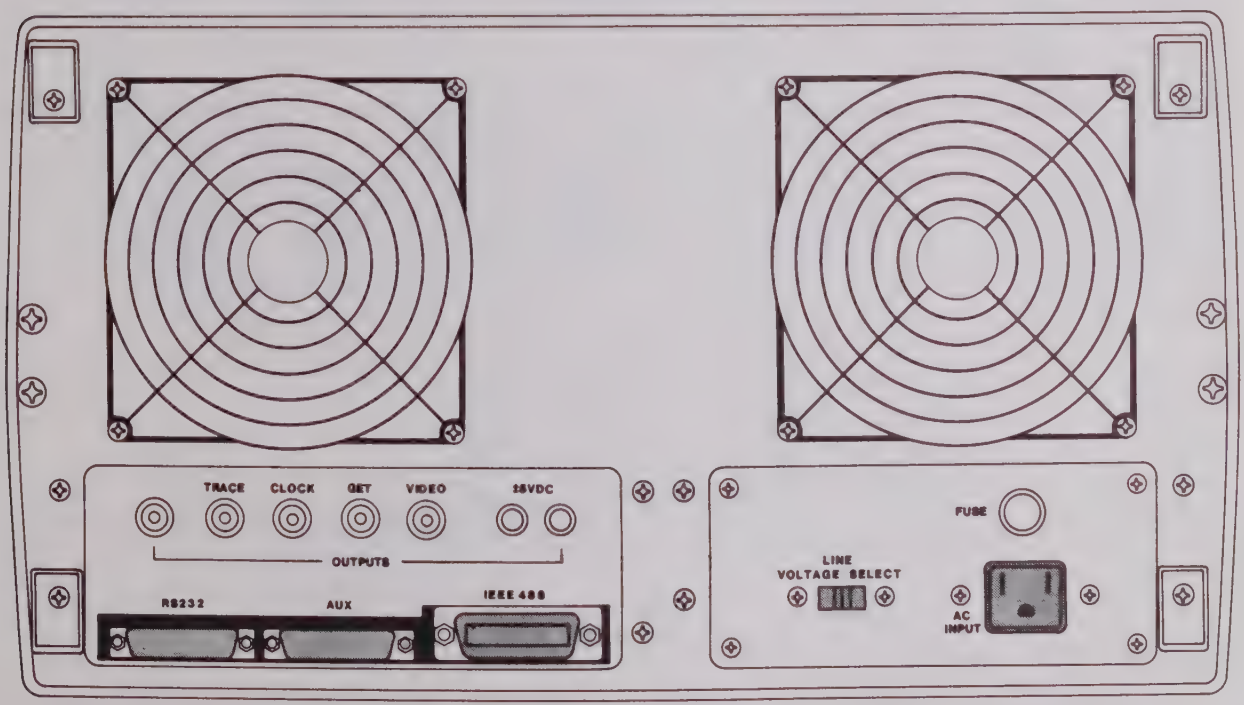


Figure 2-2. K205 Rear Panel Arrangement

- Data Display Board--The Data Display Board Assembly contains the keyboard scanning circuitry and the horizontal and vertical and high-voltage circuitry for the CRT. In addition this board contains the interface for two 5 1/4 -inch floppy disk drives and the Keyboard Assembly. This board provides an output signal to the rear panel VIDEO BNC connector.

- Clock Board--The Clock Board Assembly processes the external clocks from the probes and provides a range of internal clocks for the system. This board also provides an output signal to the rear panel CLOCK BNC connector and test pattern signal to the two front panel PROBE TEST sockets.

BOARD AND COMPONENT INTERCONNECTIONS

Boards

The K205 printed circuit boards are contained in an eight-slot card cage, and are interconnected via a mother board. Interconnection of the printed circuit boards to the front and rear connector panels is provided by flat cables that mate to connectors located along the upper edges of the board. The interface of printed circuit boards to the mother board bus and the probe inputs, as well as interaction of boards to each other and the I/O interface is shown in the block diagram of Figure 2-3.

Components

Because the K205 is a compact unit, the discrete cable harnesses necessary to connect the power supply to the mother board, and the display assembly to the Data Display Board are kept quite short. The mother board is connected to the keyboard by a short flat cable.

The optional Disk Operating System (DOS) Assembly contains the two disk drives and the associated disk controller interface board. The DOS I/O signal interface is provided by a flat cable that mates to a connector (P4) located on the Data Display Board. The power supply harness interfaces to a harness connector located on the base of the chassis. All interface cables required for the DOS installation are included with the DOS kit.

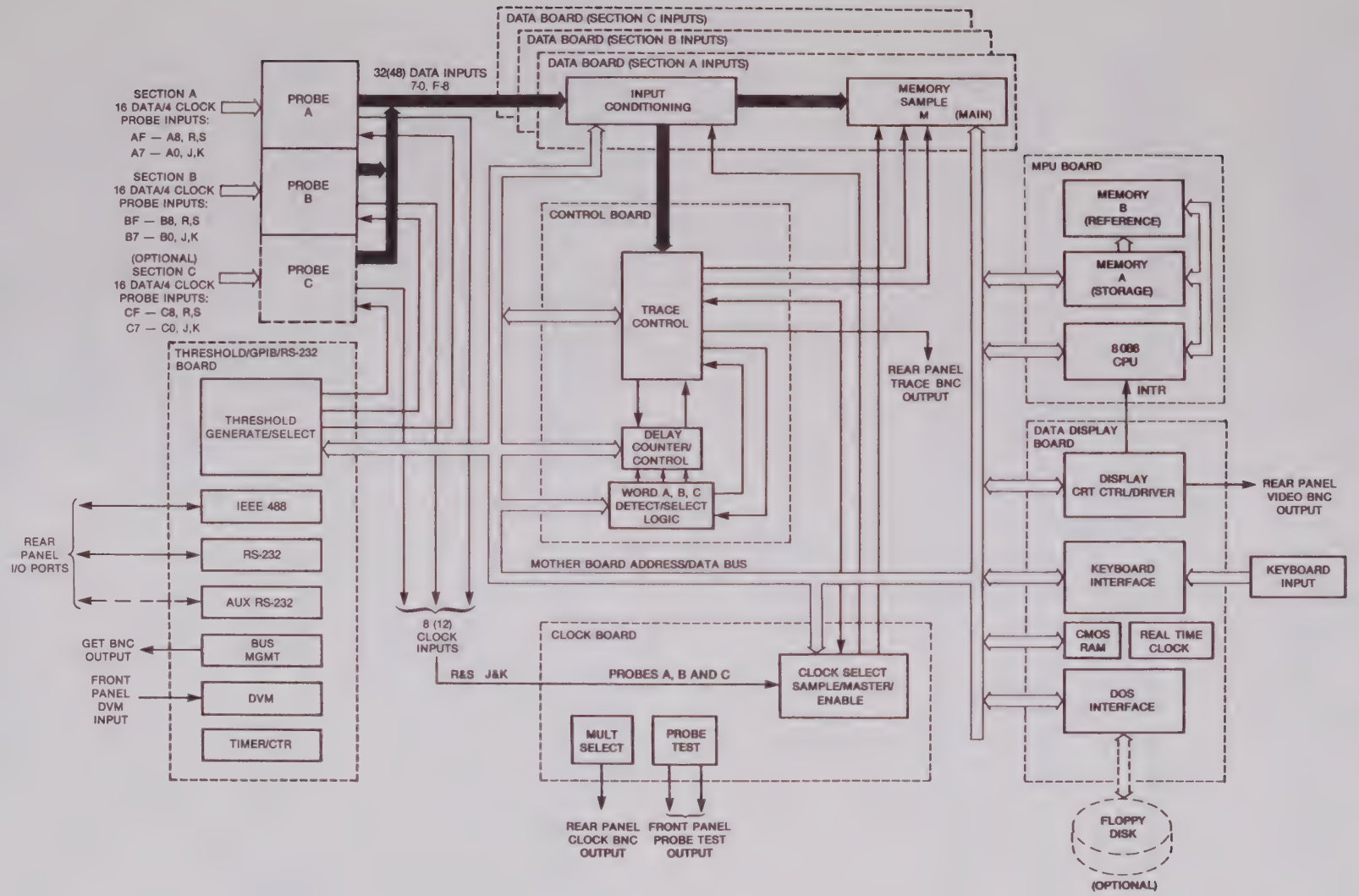


Figure 2-3. K205 System Interface of Components to Mother Board

CARD CAGE ARRANGEMENT

The K205 card cage arrangement is shown in Figure 2-4. The board ejector tabs on each printed circuit board are numbered to correspond to the assigned slot location in the card cage. For the most part, the assigned board is dedicated to reside in its assigned slot, except where noted below for the three Data Boards:

Data Board Configurations

Three Data Boards reside in slot locations A2, A3, and A4. The ejector tabs are not numbered on these boards, because each board is identical and is interchangeable for these slots. Each slot location, however, is associated with a specific SECTION INPUT as shown in Figure 2-4.

The K205 instrument configured for standard 32 data inputs (Sections A and B) uses two Data Boards installed in slot locations A4 and A3 respectively.

Instruments configured for extended 48 data inputs (Section C) use an additional Data Board installed in slot location A2.

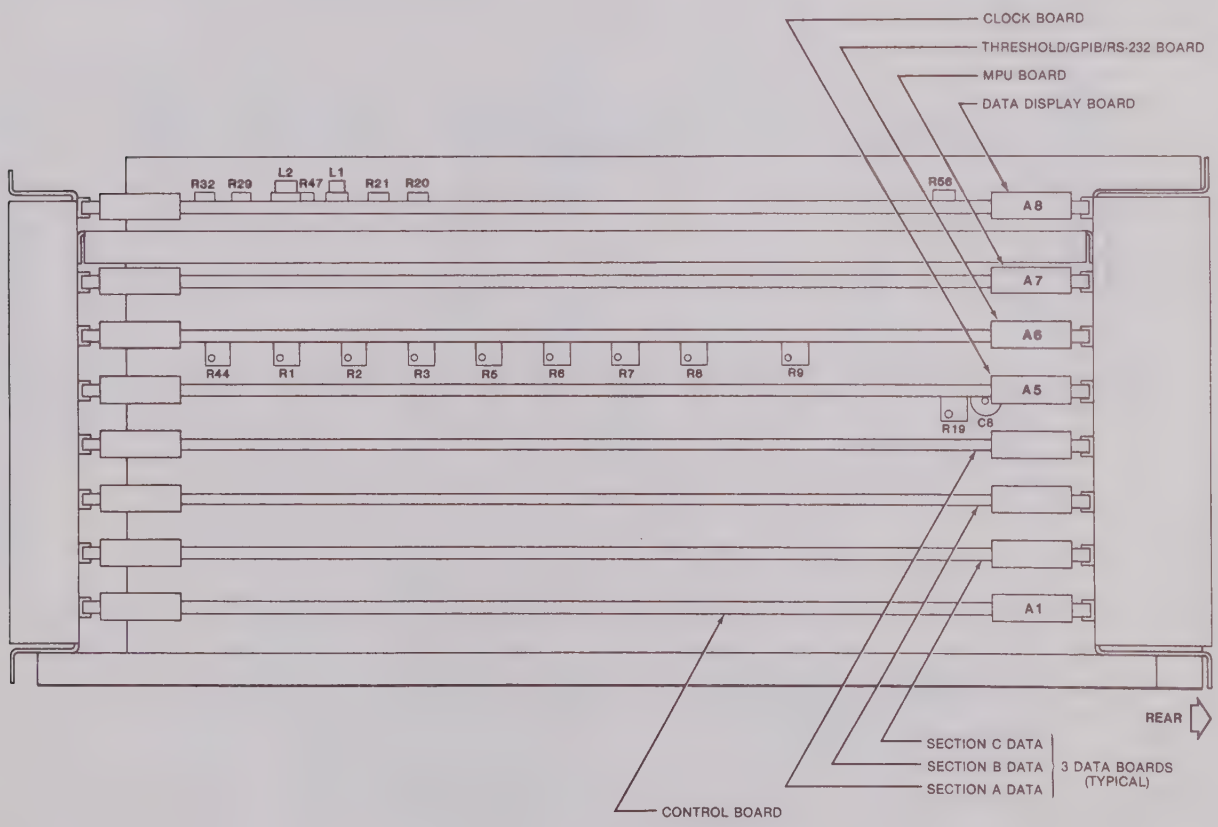


Figure 2-4. K205 Card Cage Arrangement

Board Calibration Controls

Three of the printed circuit boards, Data Display, Threshold/GPIB/RS-232, and Clock contain controls for calibrating various circuit functions. The location of these controls for a respective board is shown in Figure 2-4. The procedure for performing the calibration adjustments is described in Chapter 3. The following circuit functions are adjusted by these controls:

CARD CAGE LOCATION	BOARD NAME	CIRCUIT FUNCTION ADJUSTMENT
A8	Data Display	R20, CRT Vertical Height R21, CRT Vertical Hold R29, CRT Focus R32, CRT Brightness R47, CRT Vertical Linearity R56, Audio Alarm Volume L1, CRT Horizontal Width L2, CRT Horizontal Linearity
A6	Threshold/GPIB/RS-232	R1, R2, Variable B Threshold R3, R5, DVM Voltage R6, R9, Variable A Threshold R7, ECL Threshold R8, TTL Threshold R44, Reference Voltage (+ 10V)
A5	Clock	R19, C8, Internal Clock Frequency

SUGGESTED TEST EQUIPMENT

The following is a list of the suggested test equipment for servicing and troubleshooting the K205 Logic Analyzer:

ITEM	DESCRIPTION
Extender Board	Gould Part Number 0117-0195-01
Digital Multi-meter	4 1/2 Digits, DC Accuracy of +/- (0.03% of reading + 2 digits)
Frequency Counter	Capable of 0.01% accuracy on ECL at 100MHz
Oscilloscope	350 MHz band width, Horizontal Resolution to 1 ns/DIV
Logic Analyzer	Any current production model, Gould Logic Analyzer
20-Pin, 0.3" IC Clip	Standard
3 Mini Clips/Grabbers	Standard
4.7K-Ohm, 1/4 W, 5% Resister	Standard

Chapter 3

CALIBRATION AND POWER UP DIAGNOSTICS

GENERAL

This chapter describes the K205 Power Up diagnostic test routines and procedures for calibrating system components. This information is organized as follows:

- Power Up Diagnostics
- Probe Test
- Display Calibration
- Power Supply Voltage Measurements
- Threshold Voltage Calibration
- DVM Circuit Calibration
- Internal Clock Adjustment

POWER UP DIAGNOSTICS

The Power Up Diagnostic test is executed by the K205 to verify the operational readiness of hardware components whenever the instrument is powered up from a cold start or restarted. The power up diagnostic is implemented by a resident program in the EPROM firmware located on the MPU printed circuit board.

Diagnostic Operation

As soon as the AC POWER switch is turned ON, the K205 will beep and begin executing the diagnostic test routines. As each test is completed, the next test is automatically run. When all tests are successfully completed, the Configuration screen displays the current hardware configuration and the instrument can accept user inputs.

The power up diagnostic is also initiated when the SHIFT and DEFAULT keys are depressed to reset system operations. The power up diagnostic runs for approximately ten seconds to check for the presence of certain components and perform a series of tests. The following tests and checks are performed by the power up diagnostics:

Microprocessor RAM Test
Microprocessor ROM Checksum Test
Keyboard Stuck Key Test
Voltage Test
Display Board CMOS RAM Test
Threshold/GPIB/RS-232 Board Check
DOS Recognition Check
Data Board Recognition Check
Clock Board Recognition Check
Control Board Recognition Check

User Interaction

If an error is detected in any of the tests, the name of the failed test is displayed and further testing is halted. To run the remaining power up tests, or to attempt operation of the instrument despite the error condition, depress the NEXT key to resume testing, or depress the PREVIOUS key to repeat the test. After the last test is executed, the Configuration screen is displayed. At this point, since an error has been detected, the appropriate disk-based diagnostic test may be executed to further isolate the cause of the error.

As each power up diagnostic test is executed, the name of the test is displayed on the CRT. If the test is run successfully, the word PASSED is printed after the test name. The first failure encountered in a test is indicated by the word FAILED, which is printed after the test name. A test-results header is then printed on the next line and the results of the test are printed on subsequent lines. Any additional failures associated with the specified test name causes the results to be printed on successive lines. A detailed description of the various diagnostic tests is given in subsequent paragraphs.

Microprocessor RAM Test Description

The Microprocessor RAM Test is executed by writing and reading bits in a test pattern as follows:

1. Write 0000 to address locations 0000-FFFF.

2. Read 0000 from address locations FFFF-0000 and write FFFF at each location.

3. Read FFFF from address locations 0000-FFFF and write 0000 at each location.

4. Read 0000 from address locations 0000-FFFF and write FFFF at each location.

5. Read FFFF from address location FFFF-0000 and write 0000 at each location.

The above test is repeated, changing the segment registers so that RAM address locations 0:0000 to 3000:FFFF are all tested. If all test patterns are read back successfully, the following information is displayed:

MICROPROCESSOR RAM TEST - PASSED

If any bits fail, the following information is displayed in graphic form:

```
MICROPROCESSOR RAM TEST -              FAILED

   MPU MEMORY FAILURE

MAP OF RAMS ON MPU BOARD (G = GOOD,  X = BAD)

COL-->   3   4   5   6
ROW
  |  A   G   G   G   X
  ↓  B   G   G   G   G
     C   G   G   G   G
     D   G   G   G   G
     E   G   G   G   X
     F   G   G   G   G
     G   G   G   G   G
     H   G   G   G   G

Please press NEXT to continue.  PREV to repeat.

Where:  COL and ROW positions correspond to
        respective RAM socket locations on
        MPU board.
```

Microprocessor ROM Checksum Test Description

The ROM Checksum Test computes 16-bit checksums for each of the ROMs which are numbered from 1 to 16. The computed checksum values are then compared with the expected values which are stored in the top of ROMs 15 and 16.

If the values match, the test is successful and the system proceeds to the next test.

If the values do not match, the error display indicates the ROM number, the expected checksum value, and the actual checksum value as shown below. Note that a missing ROM generates the following display:

```
ROM CHECKSUM TEST       FAILED

  ROM        EXPECTED     ACTUAL
 NUMBER      CHECKSUM    CHECKSUM

   2          463B       ALL "FF"
```

Keyboard Stuck Key Test Description

This test performs a check of the keyboard matrix for stuck keys (i.e., where the key contacts do not make and break properly).

If one or more keys are stuck, the affected key(s) is displayed below the test failed message in a matrix that is continuously updated.

If all keys were stuck, the following information is displayed on the CRT screen:

KEYBOARD STUCK KEY TEST - FAILED

NE	^	>	CN	SH	IO	ED	AR
PR	<	v	RF	HL	SP	IN	ST
FO	MA	MB	C	D	E	F	F1
CL	DA	AB	8	9	A	B	F2
TR	TI	SE	4	5	6	7	F3
AM	GR	CM	0	1	2	3	F4

When all keys are unstuck, the test is successful and the system proceeds to the next test.

Voltage Test Description

The following voltages are checked by the power up diagnostic:

+15.00 VDC
-15.00 VDC
-10.00 VDC
+ 5.04 VDC
- 5.28 VDC
- 2.08 VDC
V BATT

Tolerance for +15V test has been arbitrarily set to +0.5 VDC. The tolerances for remaining voltages have been set to +/- 10%. The testing sequence is conducted as follows:

1. The +15V test is repeated up to 100 times. If the voltage returned is not within the tolerance limit on or before test 100 occurs, the test has failed.

2. If the +15V test is successful, remaining voltages are tested. A failed condition occurs if any of the voltages are not within acceptable limits.

3. For each voltage that fails, the following information is displayed on the CRT: name of voltage being tested, the minimum voltage limit, the maximum voltage limit, and measured voltage value(average and peak-to-peak) which was read.

Display Board CMOS RAM Test Description

The CMOS RAM is backed up by batteries to store setup parameters for recording information. This test routine causes the stored data to be compared with a checksum value which is also stored in the CMOS RAM. A failure causes an error message, as follows, to be displayed:

CMOS RAM TEST FAILED

An error condition generally indicates the instrument will not properly restore the recording setup parameters which were previously stored, nor correctly save new parameters.

The presence of an error condition, however, does not always indicate a component has failed. The source of failure could be an intermittent, soft error. Depressing the NEXT key resumes execution of the diagnostic. If the original error was not caused by a component failure, the CMOS RAM TEST ERROR should not appear on the next power up and the CMOS memory should operate correctly.

PROBE TEST

Two front panel connectors, labeled PROBE TEST, are used to quickly check the probe circuitry to verify it is operational. The test is performed on eight sample data input signals of each probe.

NOTE: The clocks are not checked by this test.

Probe Test Pattern Generator

The Probe Test Pattern Generator is always enabled. The pattern generator circuits generate an output signal to the PROBE TEST sockets consisting of a known ring-counter loop and clocking sequence. The pattern generator outputs two clock signals and eight data signals for each PROBE TEST socket. These signals are supplied as input to the probe tip.

The clock and data signals output from the PROBE TEST sockets have a voltage swing from 0 to -5 volts.

Probe Connections

The arrangement of two PROBE TEST sockets allows the low order (bits 7-0) probe and high order (bits F-8) probe of each input section to be tested concurrently. In order to avoid the possibility of extraneous noise pulses at the other input sections, it is recommended that the probe cables also be connected to these input sections while conducting the probe test. Use the following procedure to connect the probe cables:

1. Connect the low order bit probe cable to lower front panel socket labeled SECTION A INPUTS (J, K, 7-0).

2. Connect the high order bit probe cable to upper front panel socket labeled SECTION A INPUTS (R, S, F-8).

3. Repeat Steps 1 and 2 to connect probe cables to front panel sockets at Section Inputs B and C.

4. Plug the lower order bit probe tip of SECTION A INPUT cable into the lower PROBE TEST socket. Ensure label faces upward.

5. Plug the high order bit probe tip of SECTION A INPUT cable into the upper PROBE TEST socket. Ensure label faces upward.

Default Setup

The K205 contains CMOS memory which is backed up by battery to retain the previous set-up parameters. Whenever the unit is powered up from a cold start, the previous set-up parameters are restored. It is, therefore, necessary to initialize all set-up parameters to their default value as follows:

1. Depress the SHIFT and ARM MODE/DEFAULT keys to select the Configuration Screen.

2. Depress Function key, F1, to select the Default Setup Parameters.

3. Observe the following message is displayed at the top of the screen:

   Default Setup M and Display values locked in . . .

Fixed ECL Threshold Setup

1. Depress the FORMAT key; observe the Format Display indicates Data Inputs for AF through A0 and Threshold at TTL level.

2. Change the threshold for inputs AF through A0 to ECL by moving the blinking cursor to the AF-A8 line of the Data Inputs display and change TTL to ECL as follows:

   a) Depress Function key, F1, to select top of threshold.

   b) Depress FIELD down-arrow key four times to move cursor downward to AF-A8 line.

   c) Depress alphanumeric key, 1, two times to change entries to ECL level at lines AF-A8 and A7-A0.

Record/Review Test Results

1. Depress the ARM key to initiate a recording.

2. Observe the machine status message which is located in the lower right area of the screen. This status indicates a recording has occurred with the following condition:

   READY - Ready for an ARM signal
   BUSY - Setup internally for a recording
   EOR - End of recording activity

NOTE: The actual recording occurs quickly; if necessary, depress the ARM key again to view the display. Depress the F1 key to scroll through the input displays until the desired input signals are displayed on the screen.

3. Depress the TIMING key and observe the display pattern. A staircase pattern of pulses (shown in Figure 3-1) should appear on the screen. This pattern may begin at any point on the screen as determined by the Default Setup. Memory is filled with samples starting at Location 0 in the data stream.

4. Use the Control and Reference cursors to measure the characteristic total trace time of 10 microseconds and pulse width of 0.9 microsecond. The presence of these conditions indicates the probes under test are functioning properly to accept inputs for recording.

   Verify a pulse is present for each channel. If a channel does not contain a pulse, reverse the upper and lower probes and repeat the test. A malfunction of the generator can be isolated by swapping the probes. A malfunction of the probe can be isolated by swapping the probe at the input connector. If the failure is still present, the problem is associated with internal cabling or the Data Boards.

5. Repeat the Probe Test for Section B and C Inputs, and verify these probes are functioning properly to accept inputs for recording.

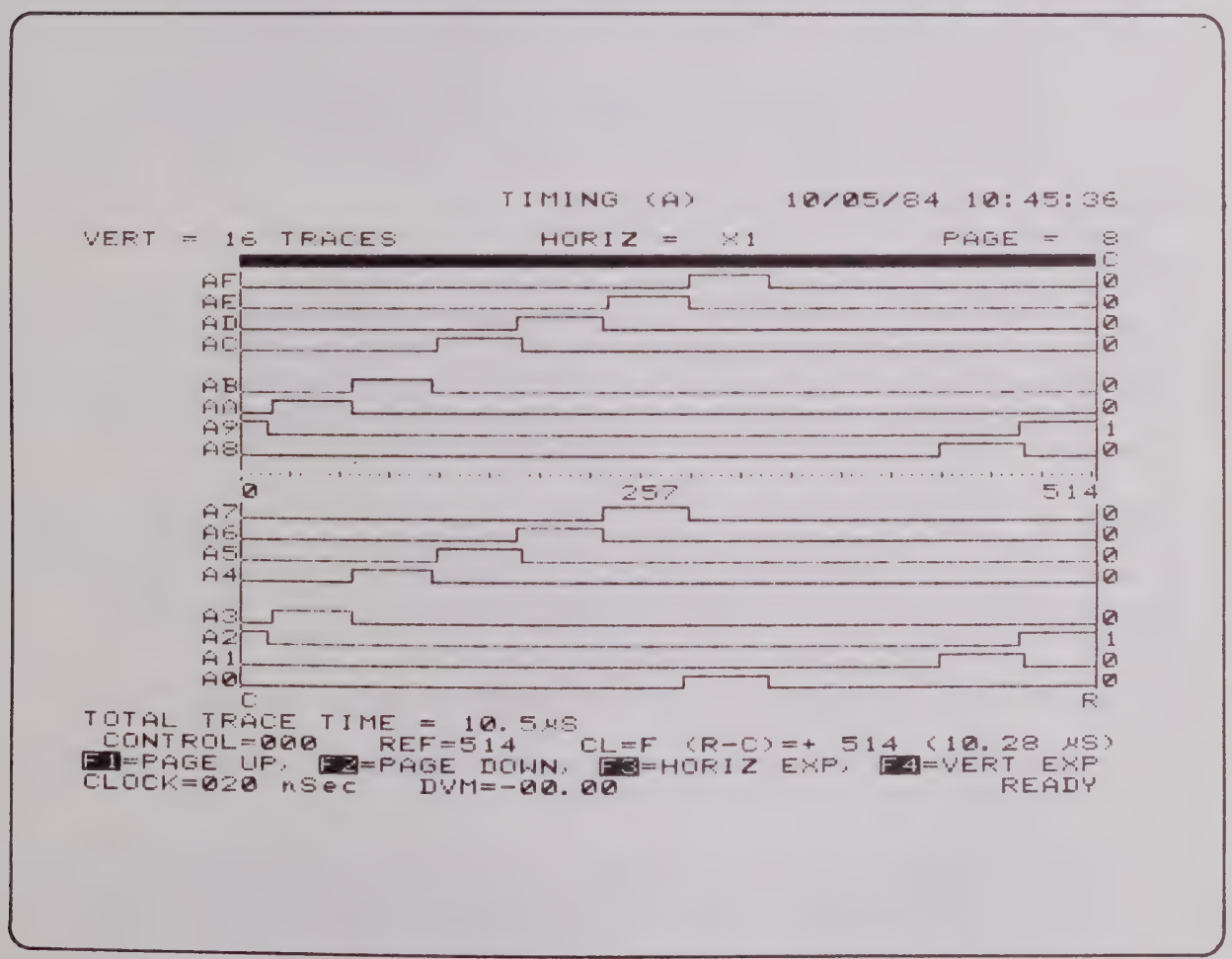


Figure 3-1. Typical Probe Test Recording Using ECL Threshold

DISPLAY CALIBRATION

The Display Board contains circuitry for generating signals that are used for driving the CRT, reading front panel Keyboard, controlling priorities for interrupt levels, controlling the Real Time Clock and driving the Audio Error Alarm.

```
* * * * * * * * * * * * * * * * * * * * * *
*                 WARNING                   *
*                                           *
*  Hazardous voltages dangerous to life     *
*  are present on the Data Display board    *
*  and CRT.  Avoid body contact in these    *
*  areas which could result in injury.      *
* * * * * * * * * * * * * * * * * * * * * *
```

Calibration Requirements

A display calibration pattern is provided by the K205 firmware. This pattern is accessed by depressing and holding the SHIFT key while powering up the unit. Raster adjustments are made with the Data Display board fully installed in the chassis. The technician is cautioned that the calibration controls are located near an area where high-voltages are generated for operation of the CRT. Body contact with the printed ciruit board and flyback transformer should be avoided. The technician is further cautioned to use nonmetallic tools when making raster adjustments.

Display Adjustment Points

Prior to attempting any height, width or linearity adjustments, the technician must first ensure the calibration pattern is centered. Centering is accomplishyed using the intersection point of the "X" traces as a reference point and locating the point to the center of the screen by moving and centering rings on the CRT yoke (See Figure 3-2).

Because all raster adjustments are interacting, recentering the calibration pattern might be required as height, width and linearity adjustments are made. Refer to Figure 3-3 for the location of adjustment controls for VOLUME (R56), VERTICAL (R20, R21 and R47), HORIZONTAL (L1 and L2), FOCUS (R29), and BRIGHTNESS (R32).

Adjustment of the Display board is to be accomplished as follows:

1. Turn power on and verify unit passes the power-up diagnostic test by displaying the Configuration Screen.

2. During power-up test, adjust VOLUME (R56) for good sound. Depressing an illegal Key with the Error Beep on causes a brief tone to be generated. The Error Beep is turned on and off by accessing the Date screen and depressing the FIELD right arrow and NEXT keys to select the Beep parameter.

3. Adjust VERTICAL HOLD (R21) until picture locks in on screen.

   NOTE: In further screen adjustments, keep 0.25 inch margins on all four borders.

4. Adjust VERTICAL HEIGHT (R20) observing that change occurs in the height. Set for the best picture.

5. Adjust VERTICAL LINEARITY (R47) observing that change occurs in vertical linearity. Set for the best picture.

6. Adjust FOCUS (R29) observing that change occurs in focus. Set for best picture.

7. Adjust BRIGHTNESS (R32) observing that change occurs in brightness. Set for good picture brightness.

8. Adjust HORIZONTAL WIDTH (L1) observing change occurs in width. Set for good picture.

9. Adjust HORIZONTAL LINEARITY (L2) observing change occurs in horizontal linearity. Set for good picture. Turn power off.

10. Hold the SHIFT key down and turn power on. A grid pattern will appear on the CRT as shown in Figure 3-4.

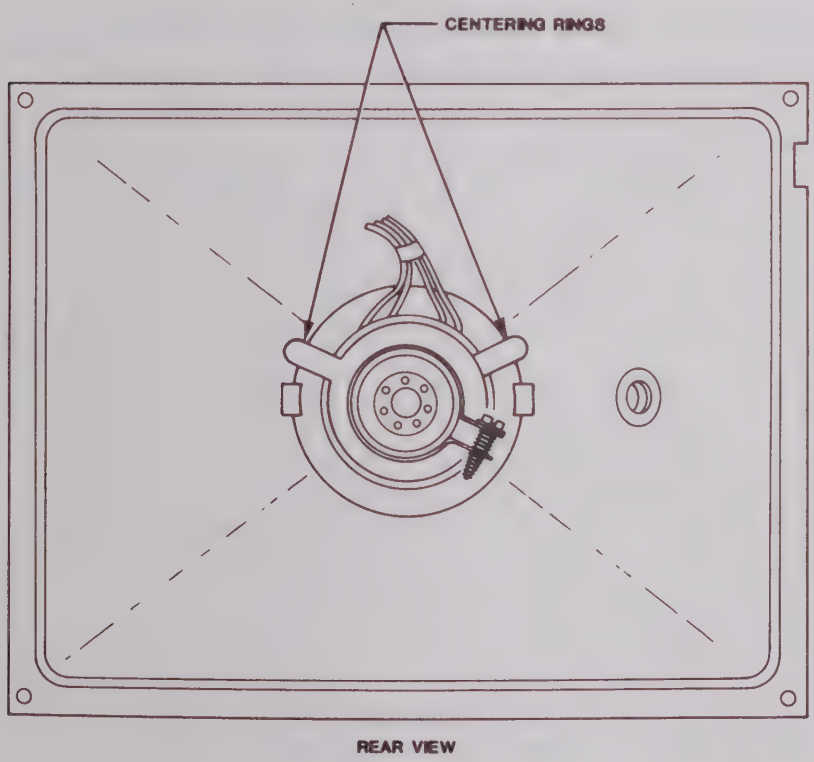


Figure 3-2. CRT Centering Rings

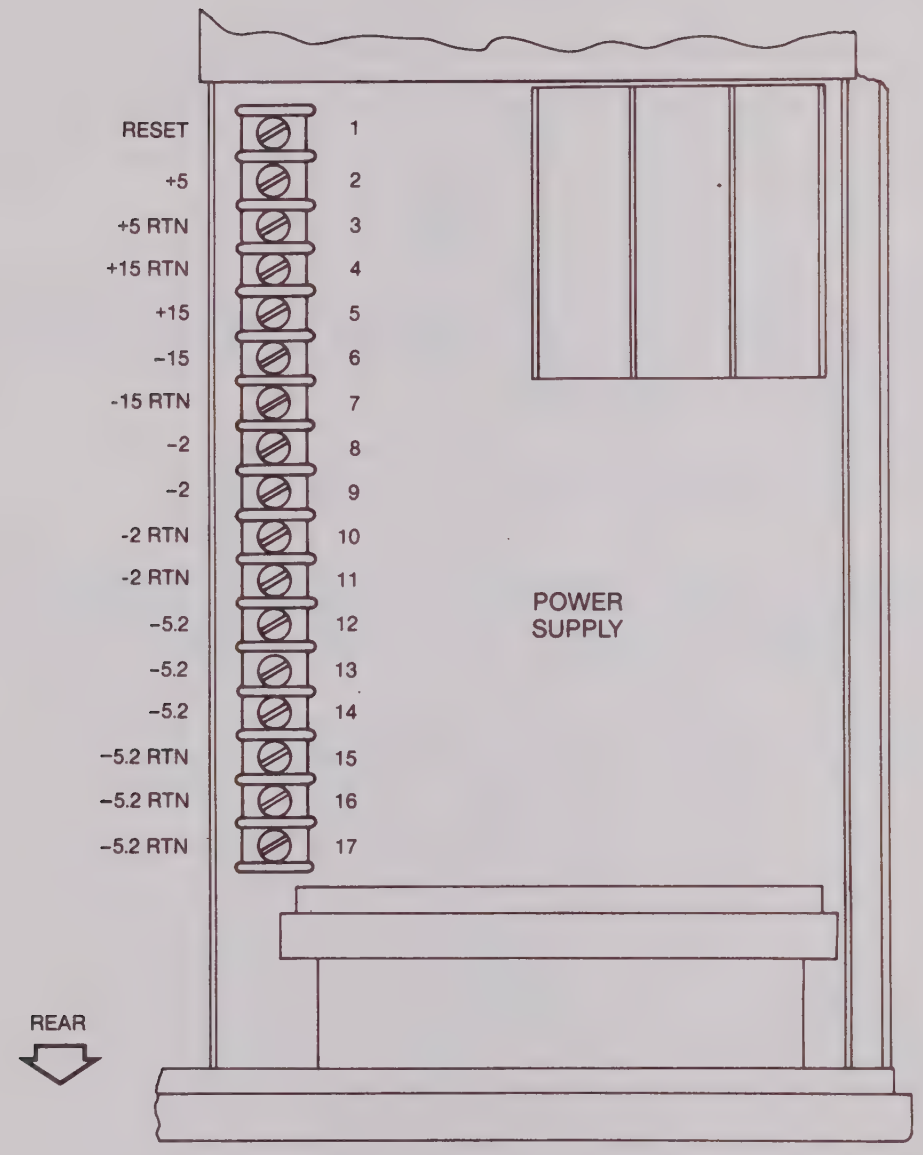


Figure 3-5. Power Supply Voltage Measurements

THRESHOLD VOLTAGE AND DVM CALIBRATION

The following adjustments are made on the Threshold/GPIB/RS-232 Board:

- 10V Reference Voltage Adjustment
- TTL Threshold Adjustment
- ECL Threshold Adjustment
- Variable A Threshold Adjustment
- Variable B Threshold Adjustment
- DVM Adjustment

The location of potentiometers to accomplish the various adjustments are shown in Figure 3-6. The following tools and test equipment are required to make these adjustments:

- Extender Board: Gould Part Number 0117-0195-01
- Digital Multimeter: 4 1/2 Digits, DC accuracy of +/- (0.03% of Reading plus 2 Digits)
- 4.7K-Ohm, 1/4 W, 5% Resistor: Standard
- External voltage source of +/- 20.000 VDC +/- 3Mv

Use the following procedures to make the adjustments:

NOTE: To ensure that proper values are set for Threshold adjustments, the user should turn the power off, then on to obtain the Configuration screen. Depressing the F1 key moves the cursor to the top Threshold location on the screen.

10V Reference Voltage Adjustment

1. Turn power off, remove the Threshold/GPIB/RS-232 Board from card cage and install on an extender board.
2. Turn power on and verify unit passes power-up diagnostic test by displaying the configuration screen.
3. Connect external DVM reference (-) to the board A GND test point, and connect the DVM (+) input to the right side of resistor R38. (These connection points are shown in Figure 3-6.)
4. Adjust R44 for a DVM reading of +10.00 +/- 0.01V.

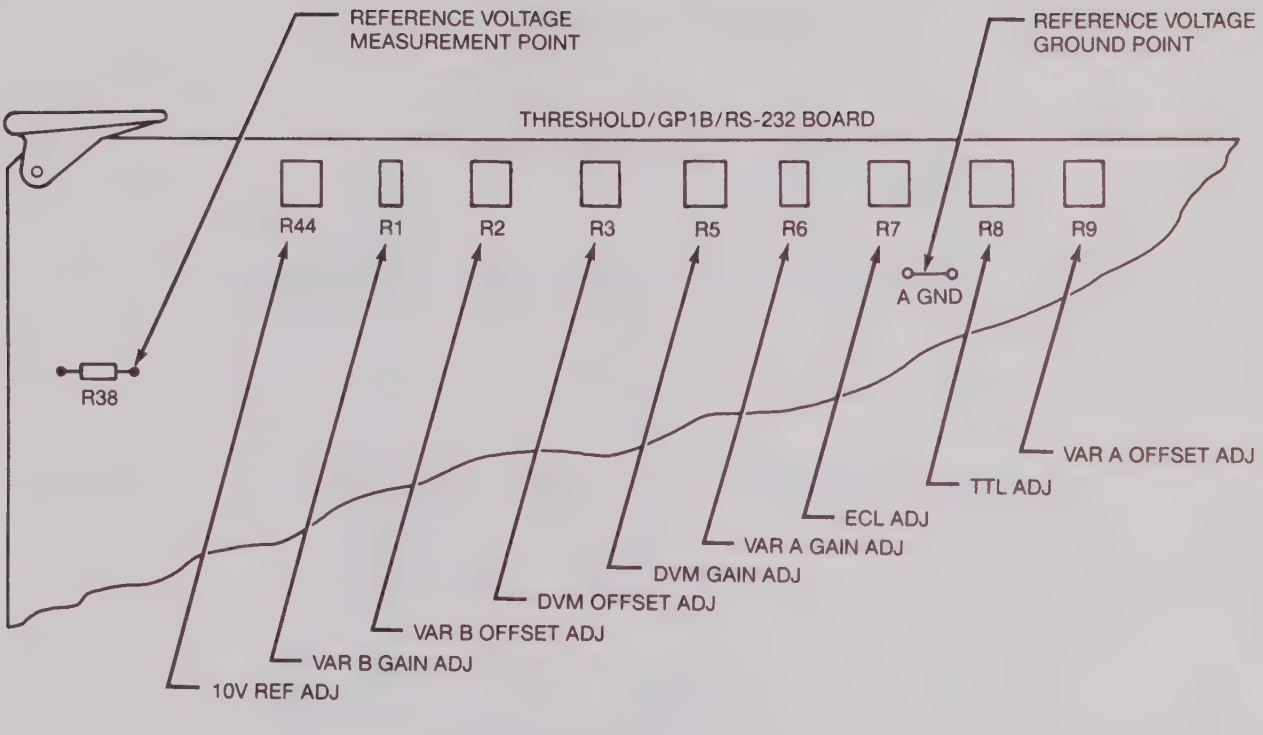


Figure 3-6. Threshold/GPIB/RS-232 Board Adjustments

TTL Threshold Adjustment

Remove all input cables from the unit. This procedure employs a 4.7K-Ohm resistor which serves as a load for adjustment of threshold voltages. All voltages will be measured accross the resistor. The TTL adjustment procedure also verifies that no shorts are present between High and Low inputs, and between Data and Clock inputs. The TTL adjustment is performed on each front panel input connector as follows:

1. Configure the K205 unit with three Data Boards to provide 16 inputs at each SECTION Input (A, B, and C).

2. Install the 4.7K-Ohm resistor between sockets 2 (ground) and 14 (Clock Threshold input) at SECTION A (bits 7-0). Connect the DVM positive (+) lead to socket 2 and DVM negative (-) lead to socket 14 so that the voltage measurement is taken across the resistor as shown in Figure 3-7.

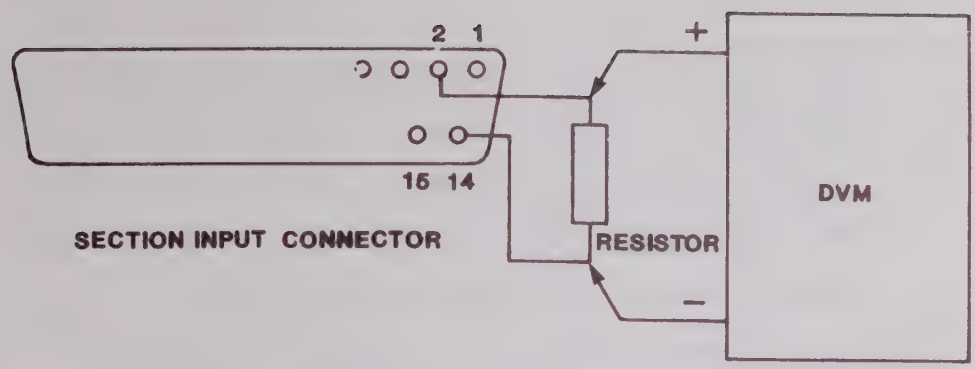


Figure 3-7. Test Connections for Threshold Voltage Adjustment

3. Depress the FORMAT Key verify that all Thresholds are set to TTL.

4. Depress the ARM key on keyboard

5. Adjust TTL THRESHOLD (R8) for a DVM reading of +1.400 +/- 5Mv.

6. Relocate the resistor to SECTION A Inputs (bits F-8) connector and verify the TTL Threshold of +1.400 +/- 25Mv is present.

7. Check the TTL level of other inputs by moving the load resistor to input connectors at SECTIONs B and C. Verify the TTL Threshold of +1.400 +/- 25Mv is present at sockets 2 and 14 of each low-byte (bits 7-0) and high-byte (bits F-8) connector.

8. Install the 4.7K-Ohm resistor between sockets 2 (ground) and 15 (Data Threshold), and repeat steps 3 through 7.

9. Ensure no shorts are present between Low and High inputs, as well as between Data and Clock inputs by performing the following test:

    a. Depress FORMAT key to select Format M screen, then depress F1 key to move cursor to top Threshold location. Depress quick key 1, to change TTL level to ECL.

    b. Move cursor down by depressing FIELD down-arrow key one time, and depress quick key 1 to change TTL level to ECL.

    c. Repeat substep b, and depress ARM key.

    d. Install the 4.7K-Ohm resistor between sockets 2 (ground) and 14 (Clock Threshold) of SECTION C upper INPUT Connector. Connect external DVM positive (+) lead to pin 2 and negative (-) lead to pin 15. Verify the ECL Threshold of -1.300V +/- 25Mv is present.

e. Install the 4.7K-Ohm resistor between pin 2 and 14 of the same connector. Connect DVM leads and verify the TTL Threshold of +1.400V +/- 25Mv is present. If the DVM reads ECL Threshold instead of TTL Threshold, this indicates a short is present between Data Input and Clock Input lines.

f. Install the resistor between pin 2 (ground) and 15 (Data Threshold) of SECTION C lower input connector. Connect DVM leads and verify TTL Threshold of +1.400V +/- 25Mv is present. If the DVM reads ECL Threshold instead of TTL Threshold, this indicates a short is present between High and Low Data Input lines.

g. Repeat substep e for this connector.

h. Repeat substeps d through f for SECTION B and SECTION A inputs.

ECL Threshold Adjustment

The ECL Threshold adjustment is performed for each front panel input connector as follows:

1. Install the 4.7K-Ohm resistor at sockets 2 and 14 of SECTION A input connector(bits 7-0). Connect the DVM positive(+) lead to socket 2 and the DVM negative(-) lead to socket 14 so that the measurement is taken across the resistor.

2. Make the following keyboard entries to change all thresholds from TTL to ECL:

   a. Depress FORMAT key to access the Format screen.

   b. Depress the FUNCTION key, F1, to move cursor to the Top Threshold location.

   c. Depress and hold quick Key 1 until ECL is selected for all threshold voltages.

   d. Depress the ARM key to change DVM reading to ECL level. ECL levels should now be selected for all inputs.

3. Adjust ECL THRESHOLD (R7) for DVM reading of +1.300 +/- 5Mv.

4. Relocate the resistor to SECTION A (bits F-8) input connector and verify the ECL Threshold of +1.300 +/- 25Mv is present.

5. Check the ECL level of other inputs by moving the load resistor to input connectors at SECTION B and SECTION C. Verify the ECL Threshold of +1.300 +/- 25Mv is present at sockets 2 and 14 of each low byte (bits 7-0) and high byte (bits F-8) input connector.

Variable A Threshold Adjustment

The Variable A Threshold adjustment is performed for each front panel input connector as follows:

1. Install the 4.7K-Ohm resistor at sockets 2 and 14 of the SECTION A Input connector (bits 7-0). Connect the DVM positive (+) lead to socket 2 and connect the DVM negative (-) lead to socket 14 so that the measurement is taken across the resistor as shown in Figure 3-7.

2. Make the following keyboard entries:

    a. Depress FORMAT key to access the Format screen.

    b. Depress the FUNCTION key, F1, to move cursor to top threshold location.

    c. Depress and hold quick Key 2 until VARA is selected for all threshold voltages.

    d. Depress the ARM key to change DVM reading to VARA level. All inputs should now indicate VARA = 9.99V.

3. Adjust VARA GAIN (R6) for DVM reading of 9.990 +/- 5Mv.

4. Make the following keyboard entries:

    a. Depress FIELD right-arrow key to move cursor right to position 9.99.

    b. Depress and hold Quick Key 0 until 9.99 inputs are set at 0.00

    c. Depress the ARM key. All inputs should now indicate VARA = 0.00V.

5. Adjust VARA OFFSET (R9) for DVM reading of 0.000 +/- 5Mv.

6. Make the following keyboard entries:

    a. Depress and hold Quick Key 9 until 0.00 inputs are set at 9.99.

    b. Depress ARM key.

7. Adjust VARA GAIN (R6) for DVM reading of +9.990 +/- 5Mv.

8. Make the following keyboard entries:

    a. Depress FIELD left-arrow key to move cursor left to the + position.

    b. Depress the NEXT key to change positive (+) to negative (-) value.

    c. Depress the ARM key.

9. Note the value of DVM reading and adjust VARA GAIN (R6) for -9.990V + 1/2 the difference of actual reading and -9.990V. (For example, if the actual DVM reading is -9.98V, subtract this value from -9.990V. The difference of -0.01V is divided by 2 to obtain -0.005V and R6 would be adjusted for -9.995V.)

10. Repeat steps 6 through 9 until the offset is the same for both positive and negative voltages within an accuracy of +/- 30Mv.

Variable B Threshold Adjustment

The Variable B Threshold adjustment is performed for each front panel input connector. The procedures are the same as steps 1 through 10 for the Variable A adjustment, except for the differences detailed in each step as follows:

1. Install the 4.7K-Ohm resistor at SECTION A input connector as described in Variable A Threshold adjustment procedure.

2. Make the following keyboard entries:

    a. Depress FORMAT key to access the Format screen.

    b. Depress FUNCTION key, F1, to move cursor to top of threshold.

    c. Depress and hold quick Key 3 until VARB is selected for all threshold voltages.

    d. Depress the ARM key to change DVM reading to VARB level. All inputs should now indicate VARB = 9.99.

3. Adjust VARB GAIN (R1) for DVM reading of 9.990 +/- 5Mv.

4. Make the following keyboard entries:

    a. Depress FIELD right-arrow key two times to move cursor right to position 9.99.

    b. Depress and hold quick Key 0 until 9.99 inputs are set at 0.00.

    c. Depress the ARM key. All inputs should now indicate VARB = +0.00V.

5. Adjust VARB OFFSET (R2) for DVM reading of 0.000 +/- 5Mv.

6. Make the following keyboard entries:

    a. Depress and hold Quick Key 9 until 0.00 inputs are set at 9.99.

    b. Depress ARM key.

7. Adjust VARB GAIN (R1) for DVM reading of +9.990 +/- 5Mv.

8. Make the following keyboard entries:

   a. Depress FIELD left-arrow key to move cursor left to the + position.

   b. Depress the NEXT key to change positive (+) to negative (-) value.

   c. Depress the ARM key.

9. Note value of DVM reading and adjust VARB GAIN (R1) for -9.990V + 1/2 the difference of actual reading and -9.990V.

10. Repeat steps 6 through 9 until the offset is the same for both positive and negative voltages within an accuracy of +/- 30Mv.

DVM Circuit Adjustment

The user must provide an external voltage source of +20.000 +/- 3Mv DC that is used to calibrate the K205 Digital Voltmeter (DVM) circuit. The adjustment controls for DVM GAIN (R5) and DVM OFFSET (R3) are located on the Threshold/GPIB/RS-232 Board shown in Figure 3-6.

The Configuration screen is used to provide the DVM readout for making the adjustments. Note that any display screen may be used to read the DVM voltage except those displays associated with Memory A or B.

Use the following procedure to calibrate the DVM circuit:

1. Turn power on and verify unit passes the power-up diagnostic test.

2. Connect DVM POS (+) lead to external DC voltage source positive output, and connect DVM NEG (-) lead to external DC negative output.

3. Set the external DC voltage source for a DVM reading of +20.000 +/- 3Mv.

4. Connect positive lead of external voltage source to the POS DVM INPUT jack located on K205 front panel, and connect negative lead of external voltage source to the NEG DVM INPUT jack on K205 front panel.

5. Check the voltage indication at the external voltage source to verify the adjusted value of +20.000 +/- 3Mv is still present. Readjust the voltage if necessary.

6. Observe the DVM value indicated on the K205 display. Adjust the DVM GAIN (R5) for a K205 DVM value of +20.00V on the display.

7. Set the external DC voltage source to indicate 0.000 +/- 3Mv and observe the DVM value indicated on the K205 display.

8. Adjust the DVM OFFSET (R3) for a K205 DVM value of 0.00V on the display.

9. Set the external DC voltage source to indicate -20.00V +/- 3Mv and observe the DVM value presented on the K205 display.

10. Verify the K205 DVM value indicates -20.00V. Adjust the DVM GAIN (R5) if necessary to obtain this reading.

11. Repeat steps 3 through 10 until the adjusted K205 DVM values of +/- 20.00V and 0.00V are obtained within the limits of +/- 3Mv.

INTERNAL CLOCK ADJUSTMENT

This adjustment is performed on the Clock Board and includes circuits that select internal and external clocks, and enable circuits.

The following tools and test equipment are required to make the clock adjustments:

- Frequency Counter: Capable of 0.01% accuracy on ECL at 100 MHz
- Oscilloscope: 350 MHz Band Width, Horizontal Resolution to 1 ns/Div
- Extender Board: Gould Part Number 0117-0195-01

Adjustment is accomplished as follows:

1. Turn power off, remove Clock Board from card cage, and install on the Extender Board.

2. Connect six cables and probes to front panel connectors at SECTION A, B, and C Inputs.

3. Turn power on and verify unit the power up diagnostic test by displaying the Configuration screen.

4. Connect oscilloscope input lead to pin 12 on IC device at board location 12C. Connect the other lead to ground lug at board location 11B (see Figure 3-8 for Clock Board component locations).

5. Connect frequency counter to pin 12 on IC device at location 12C, and ground lug at board location 11B. Adjust C8 for a frequency of 100 +/- 0.1 MHz (99.9 to 100.1 MHz).

6. Adjust oscilloscope signal for an ECL level with a symmetrically shaped waveform.

NOTE: Use R19 for making adjustment to obtain the symmetrical waveform.

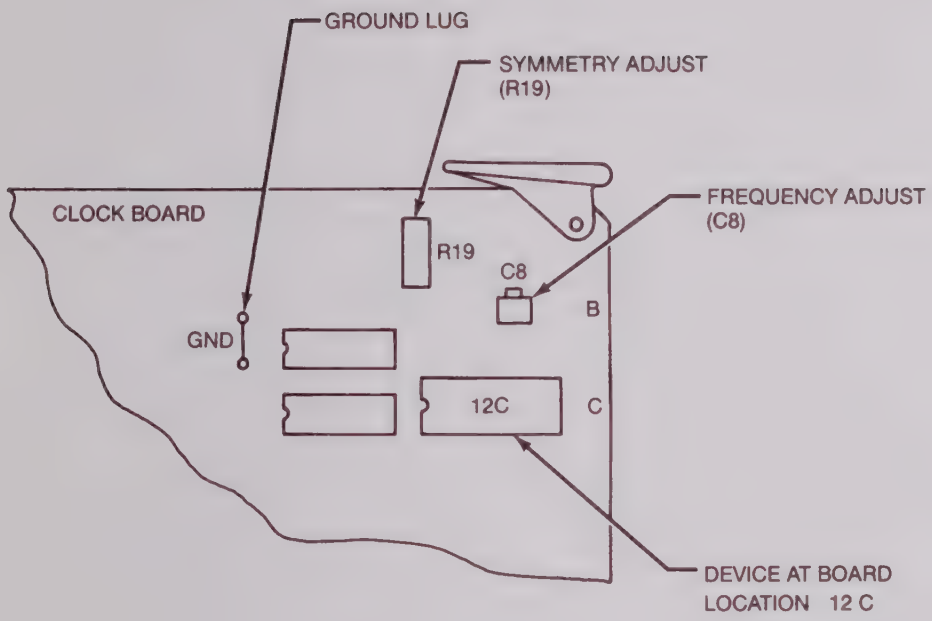


Figure 3-8. Clock Board Internal Clock Adjustment

CHAPTER 4

THEORY OF OPERATION

GENERAL

This chapter describes theory of operation for the K205 Logic Analyzer unit. An overview of the unit operation is presented initially to show the relationship and interaction of the various circuit functions. A simplified system Data Flow and Control block diagram is provided to support the overall unit description and identify major components associated with the circuit functions.

The overview is followed by a detailed description of internal circuit functions for each printed circuit board. These descriptions are referenced to specific board components and circuit functions contained in the schematic diagrams of chapter 6. A simplified block diagram of board functions is provided to support these descriptions. Theory of operation is provided for the following printed circuit boards:

- Data Display Board
- MPU Board
- Threshold/GPIB/RS-232 Board
- Clock Board
- Data Board
- Control Board

OVERVIEW OF K205 UNIT OPERATION

The block diagram of Figure 4-1 presents the overall K205 system data flow and control operations. This diagram also shows the K205 system architecture and interaction of board circuit functions.

MPU Board Interaction

The K205 Logic Analyzer employs a 16-bit, 8086 microprocessor for controlling system operations. The 8086 CPU is located on the Master Processor Unit (MPU) board. The MPU Board addresses all other boards in the system as I/O devices and communicates with the circuit boards via the multiplexed address/data bus interface on the motherboard. The operating system accommodates up to 128K bytes of ROM and 256K bytes of RAM also located on the MPU board.

The K205 operating system and power-up diagnostic routines are resident firmware programs stored in the sixteen EPROM chips located on the MPU board. This firmware executes to control the K205 operations that perform digital circuit analysis and processing of external data and clock signals supplied by the user's equipment.

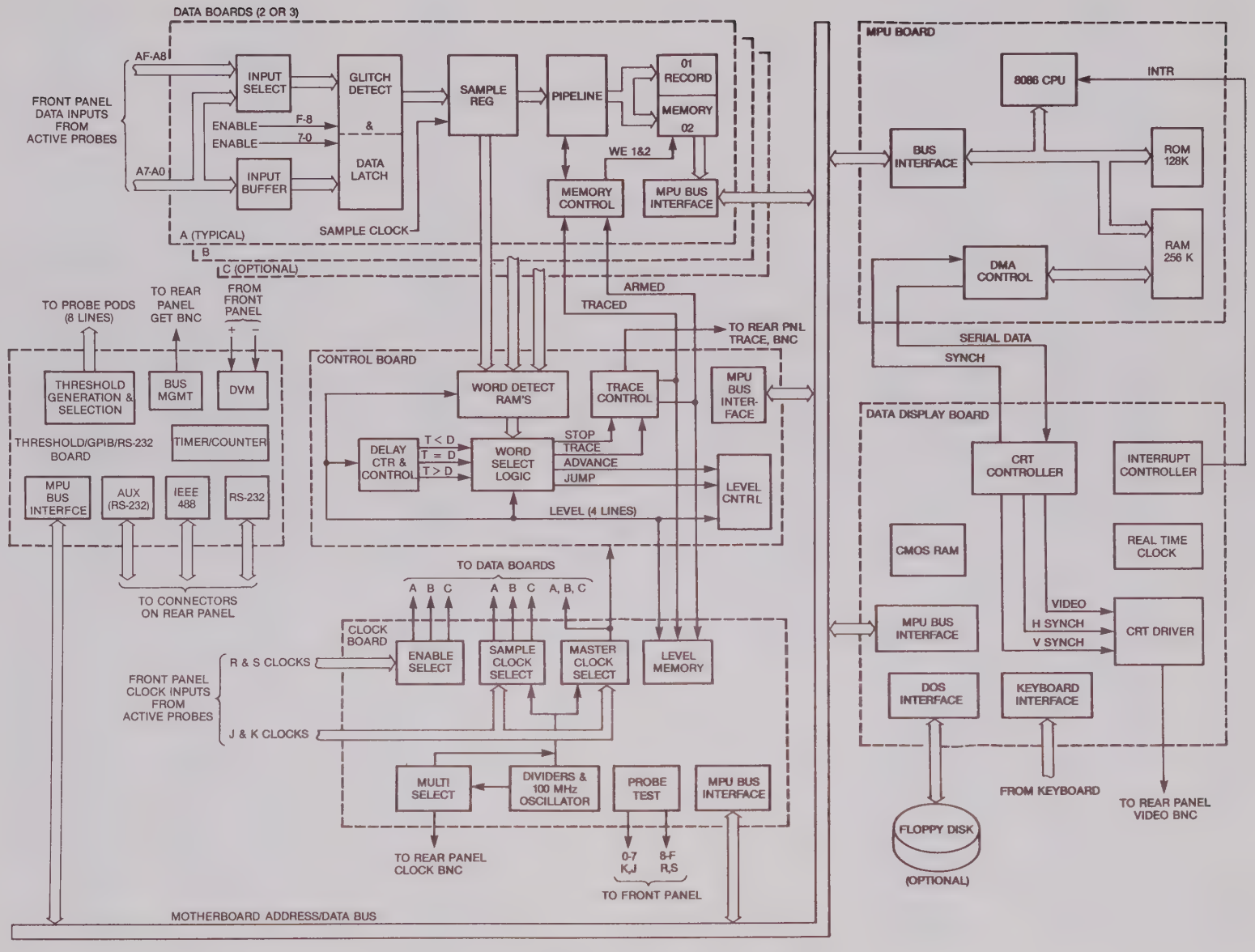


Figure 4-1. K205 System Block Diagram

Information collected and analyzed by the system is recorded in main memory where the results can be selectively accessed by the user and displayed on demand. The MPU Board provides the control functions for display, display setups, memory transfer, memory control, memory compares and keyboard input.

Data Board Interaction

The external data and clock input signals collected by the probes are supplied to the input panel. The data input signals (7-0 and F-8) are directed to the Data Board. The clock input signals (J & K and R & S) are sent to the Clock Board. The processing of data and clock inputs by various board functions to effect recording of traced information is described in subsequent paragraphs. The Data Board functions provide conditioning circuits that buffer the input data signals, select high/low bytes and detect glitches. These functions define the sample content that is directed via pipeline control circuits to main memory and word detection RAM on the Control Board. Control signals from MPU holding registers select the data source that is passed through the sampling circuitry. Input signals from the Control Board initiate the ARMED and TRACED condition so that the sample is recorded in Memory.

Clock Board Interaction

The Clock Board combines and selects clock signals to generate Latch, Sample and Master clocks. The J & K clock inputs and R & S latch inputs are combined in user defined AND/OR Boolean expressions. The internal clock is generated on this board and is always available at the CLOCK output BNC connector on the rear panel.

The 100MHz internal clock is also generated on this board. The user selected clocks and combined clocks are routed to the Data Boards and the trace Control Board. The PROBE TEST output signal at the front panel connector is generated by the pattern generator on the Clock Board.

Control Board Interaction

The Control Board contains decision making logic for control of the trace and recording process. This includes word recognition circuits that detect the sample data supplied from the Data Boards. Delay counter logic combines delay conditions with detected words to set up sequencing for Stop Recording, Jump or advance to another recording level with different parameters, and to enable or disable recording for the input sample data. The trace control logic resolves these conditions to initiate the ARMED and TRACE signals that are sent to the Data Board to enable recording of the traced information. The Control Board also generates the TRACE output signal supplied to the BNC connector on the back panel.

Threshold/GPIB/RS-232 Board Interaction

The Threshold/GPIB/RS-232 Board generates two variable, and two fixed threshold voltage sources that are supplied to the probes. The variable voltages are VAR A and VAR B; the fixed voltages are TTL and ECL. Threshold control circuits enable each probe to select one of these voltage sources. The VAR A and VAR B threshold levels are driven by software-controlled, digital-to-analog converter (DAC) circuits. A comparator circuit performs the analog-to-digital conversion (ADC) that is used by the power-up diagnostic to measure power supply voltage levels. The TTL and ECL Threshold sources use a voltage divider network and +/- 10V reference voltage for generating the fixed levels.

Both the RS-232 and AUX serial communication links are driven by a Universal Synchronous/Asynchronous Receiver/Transmit (USART) chip. The GPIB (IEEE-488) parallel interface for Talker (send) and Listen (receive) modes transfer data under control of an interrupt line. The GPIB state control circuits generate the interrupt signal that is supplied to the Data Display Board. The GPIB control circuits generate the GET (Group Execute Trigger) output signal that is supplied to the BNC connector on the rear panel. The DVM input supplied from the front panel is buffered onto the Threshold/GPIB/RS-232 Board where the analog-to-digital conversion takes place.

Data Display Board Interaction

The Data Display Board presents a display pattern that is derived by the MPU processing and stored in the RAM as a complete dot map. Each dot location of the CRT is represented by a bit in the RAM (where 1 = white, 0 = black) which is subsequently supplied to video control circuits on the Data Display Board. The video control circuits accept CRT address clocking information and serial input data supplied by the MPU and generates the video control signals that drive the horizontal, vertical, and synchronization for the CRT. The CRT controller circuits continuously interact with processor circuits to generate direct memory access cycles from the RAM and translates this information to the CRT. A 16-bit word is read from the RAM every 2 us and converted into a string of 16 dots on the CRT.

The Data Display Board also accepts interrupt signals generated by other board circuits. The interrupt signals are used by the Data Display Board interrupt processor to send an interrupt to the MPU.

The Data Display Board provides the Keyboard interface and DOS interface. The Real Time Clock and CMOS Memory Save circuits are backed up by battery power which continues to drive these circuits when facility power is interrupted or removed from the K205 unit. The Audio Error Alarm circuit is also contained on the Data Display Board.

DATA DISPLAY BOARD OPERATIONS

Overview

This section describes Theory of Operation for the K205 Data Display Board assembly, Part Number 0114-2010-40. The board assembly drawing, schematic diagrams and list of material are provided in Chapter 6. Reference is made to the schematic diagrams throughout the descriptions of circuit functions. The Data Display Board block diagram is shown in Figure 4-2. The following board circuit functions are described in subsequent paragraphs:

- CRT Controller (Schematic sheets 1, 2 and 3)
- Interrupt Processor (Schematic Sheet 4)
- Keyboard and Front Panel Interface Circuit (Schematic Sheet 4)
- CMOS RAM Save Circuit (Schematic Sheet 5)
- Audio Error Alarm Circuit (Schematic Sheet 4)
- Real Time Clock (Schematic Sheet 6)
- DOS Interface Circuit (Schematic Sheet 6)

CRT Controller

The CRT Controller circuit (sheet 3 of schematic diagrams) generates a standard raster scan display format with data presented as a series of horizontally scanned lines. Each line starts at the left of the screen and goes to the right. The first line is at the top of the screen and the last is at the bottom. Standard sync and blanking signals are generated. The K205 operates at a 50Hz scan rate at all times.

Horizontal Timing: Each horizontal scan line is 64 usec long and presents 52 usec of video with 12 usec blanked and a 6-usec sync pulse during the blank time. The LS161 Horizontal Counter at location 9A and 10A runs continuously at a 500 KHz rate generating the five address lines for the horizontal ROM at 10B. The Horizontal ROM decodes the address to produce the blanking, sync and top count (end-of-line) pulses (74LS175 location 9B). The horizontal blanking interval occurs for the first 12 usec after the counter rolls over, states 0 through 5 (pin 7 of 9B). The sync pulse at pin 3 of 9B starts 2 usec after the blanking and lasts for 6 usec. In addition to addressing the ROM, the fifth address line is used by the horizontal drive for the deflection (pin 10, location 10C).

Vertical Timing: The vertical timing cycle begins with counters preset to 7200 Hex. The horizontal and vertical PROMs decode top count after counting 290 lines, and reset the counter to 7200 Hex. Simultaneously with the vertical top count, the vertical PROM generates the PRESET ADDRESS COUNTER signal which synchronizes the tracking address counter on the MPU board. The The vertical sync pulse is decoded to occur at line 35 Hex.

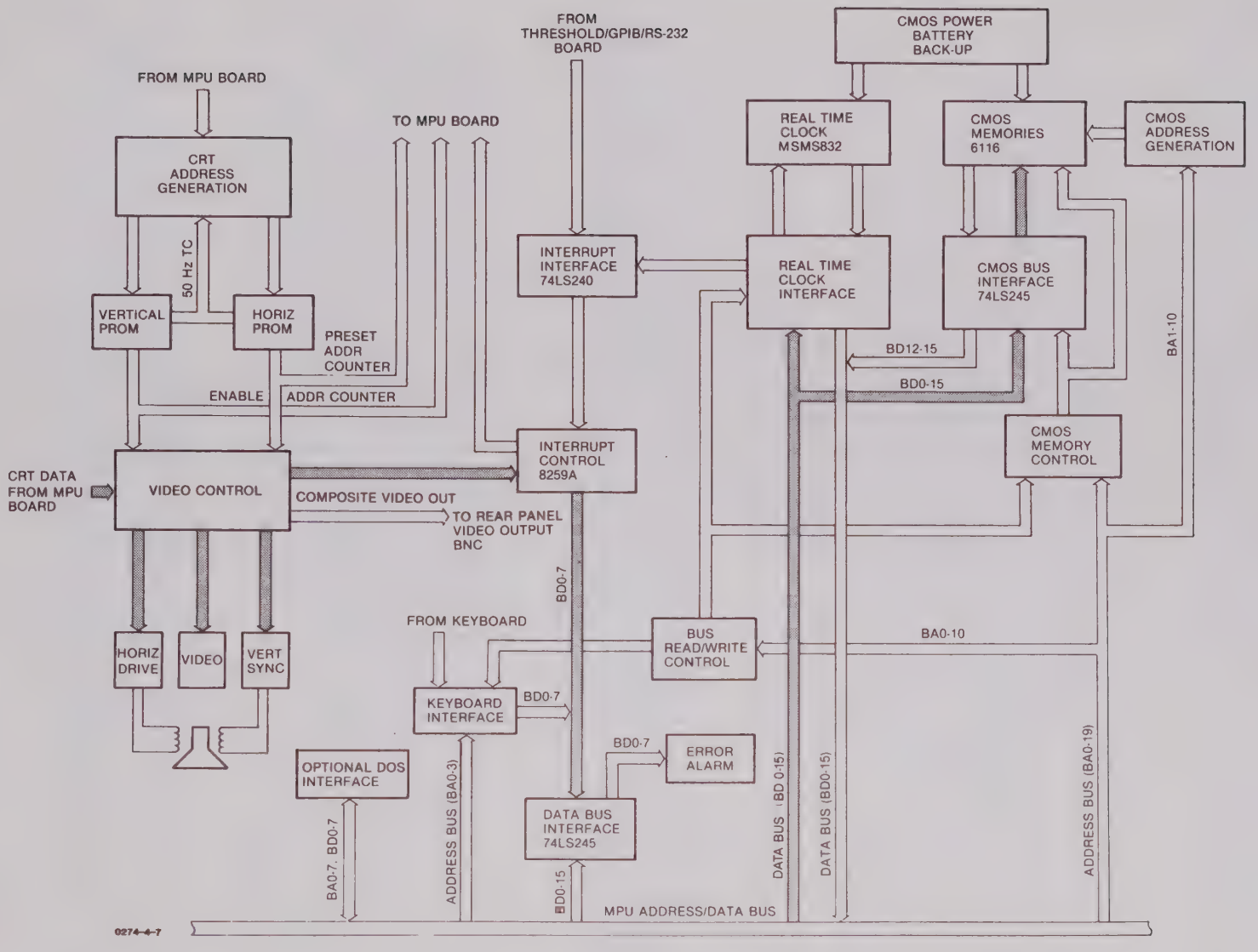


Figure 4-2. K205 Data Display Board Block Diagram

Horizontal Deflection and High Voltage: The horizontal drive signal from the CRT controller synchronizes the horizontal scanning with the retrace blanking by controlling the horizontal drive transistor, Q5 (sheet 1 of schematic diagrams). The horizontal drive transistor (Q5) performs two functions; it provides energy to the flyback transformer and it draws current from the horizontal deflection coil to generate the scan from left to right. The Flyback Transformer, T2 provides the energy for rapid retrace from right to left and it serves as an AC to DC converter for generating the operating voltages for the CRT. The following voltages are supplied to the CRT:

+10KV	CRT Anode
+200V	Focus
+30V	Cathode
-40V	CRT Grid

The horizontal deflection and high voltage circuit allows adjustment of the Focus (R29) and Brightness (R32) which are located near the top of the board. The Horizontal Width adjustment (L1) and Linearity adjustment (L2) are also present.

Vertical Deflection: The vertical processor (sheet 2 of schematic diagrams) generates and synchronizes the vertical scanning. The vertical processor drives the vertical deflection coil directly, and senses current through the coil via a sense resistor. The TDA 1270 processor (11B) contains an oscillator that is synchronized to the vertical sync pulse, an adjustable constant current source ramp generator, an emitter follower, and a power amplifier to drive the coil. The vertical processor circuitry allows adjustment of Vertical Hold (R21) Vertical Height (R20) and Vertical Linearity (R47).

Video: The CRT brightness is controlled by combining the digital data with the horizontal and vertical blanking signals and switching the cathode voltage between zero volts (white) and +30V (black). The video is modulated by an 8MHz clock signal to provide a sharper display presentation. A composite video signal is also generated at the rear panel BNC connector for use with another video monitor.

Video Operation: Transistor Q3 operates as the video amplifier and applies the video signal to the cathode of the CRT. R28 is the load resistor connecting Q3 to the 30 VDC supply. The 30 VDC supply is composed of CR6 and C38, and the -40 VDC grid bias supply for the CRT consists of CR3 and C35. CR4 and C37 comprise the 200 VDC focus electrode supply.

The source voltage for these supplies is the high-voltage transformer, T2. Note also that T2 supplies the 10 KV for the second-anode of the CRT. The rectifier for the high-voltage is an integral part of the second-anode lead, and the filter capacitor for the high-voltage is the 600pF capacitance of the CRT aquedag coatings.

Transformer T1 and transistors Q4 and Q5 drive transformer T2: When Q5 is conducting, energy is stored in the primary of T2. When Q5 is switched off, the energy stored in the T2 primary is transferred to the secondary.

When Q5 switches off, the voltage at its collector rises to approximately 120 VDC and is impressed upon the horizontal deflection coil via L1 and L2. This voltage causes a current to flow in the deflection coil which in turn causes the electron to deflect to the left side of the CRT. The positive current flow decays in a linear manner, being zero at center screen. Because of the resonant circuit, C53 and the deflection coil, the current increases in the negative direction for the right side of the screen. At center screen Q5 again switches on and remains on until the beam is deflected to the right side of the screen. At this time, Q5 again switches off, and the process begins again.

Vertical deflection is accomplished using a TDA1270 integrated circuit, U11B. This IC contains an oscillator, a preamp and a power amp. The oscillator frequency is controlled by R21, R22 and C49. The waveform is shaped by R20, R37, R42, R44, R47, C45 and C46. The waveform is amplified by the preamp and power amplifier and impressed upon the vertical deflection coil via C51. The current is sensed across R45 and returned to the preamp via feedback resistor R46.

Interrupt Processor

The Interrupt Processor circuit (sheet 4 of schematic diagrams) accommodates up to eight levels of interrupts (INT0 - INT7) using a 8259A Interrupt Processor chip (2E). Seven levels of interrupts are used for K205 application with the following assignments:

INTERRUPT LEVEL	ASSIGNMENT
INT7	Floppy Disk Controller
INT6	1 Second (Time of Day Clock)
INT5	(Not used)
INT4	Timer #0
INT3	Auxiliary, RS-232 (USART#2)(RXRDY+TXRDY)
INT2	RS-232 (USART #1) (RXRDY+TXRDY)
INT1	GPIB
INT0	50Hz (CRT Interrupt)

Keyboard and Front Panel Interface Circuit

The Keyboard and Front Panel Interface (sheet 4 of schematic diagrams) are addressed simultaneously by the microprocessor. The interface circuit decodes eight addresses out of the I/O map. Each row is read as a byte at 50Hz rate. Any key contact that is closed is stored as a zero within the selected byte. Each bit of the byte corresponds to a column on the keyboard.

CMOS RAM Save Circuit

The CMOS RAM Save circuit (sheet 5 of schematic diagrams) provides 2K x 16 memory storage. If the k205 unit is powered down, the save circuit will automatically store the last parameters displayed on the screen.

A 2.9V battery (location B1) provides power to the two 6116 CMOS RAMs and the Real Time Clock when the unit is powered down. Data to and from the 6116 RAMs is transferred over a bi-directional data bus via the two 74LS245 Three-State Transceivers at locations 3C and 4C.

Real Time Clock

The Real Time Clock circuit (sheet 6 of schematic diagrams) is controlled by the MSM5832 IC module (location 2D) which drives the real time clock. A 32.768 KHz crystal (location Y1) is used to generate the clock frequency. The variable capacitor (C10) provides for adjustment of the frequency. The adjustment of C10 is set by the factory and is not available to the user. The clock is set by the software via the Date and Time Set Up display.

Audio Error Alarm Circuit

The Audio Error Alarm circuit (sheet 4 of schematic diagram) produces a low level beep tone when improper keyboard entries are made. The tone volume is controlled by R56. Enabling and disabling the tone is controlled by software selection via the Date and Time setup display.

DOS Interface Circuit

The optional DOS Assembly contains the Floppy Disk Controller board which communicates with the K205 via a signal cable link. The connector P4 on the Data Display Board (sheet 6 of schematic diagrams) provides the I/O link for the DOS Assembly. Information for Address (BA0-BA7) and Data (BD0-BD7) is supplied from P4 to the MPU Address/Data Bus on the motherboard via the P15 and P16 edge connectors. The Interrupt control (INTR 7) signal is supplied to the 8259A Interrupt Processor (location 2E, sheet 4 of schematic diagram) where it is then directed to the MPU via the control bus.

MPU BOARD OPERATIONS

Overview

This section describes theory of operation for the K205 MPU Board, Part Number 0114-0185-80. The circuits on the MPU Board consist of an 8086 microprocessor, address registers, data transceivers, random access memory (RAM), read only memory (ROM), memory controller and I/O decoder. This board provides control functions for display, display setups, memory transfer, memory functions, memory compares and keyboard.

The MPU Board block diagram is shown in Figure 4-3. The associated assembly drawing, schematic diagrams and list of materials are provided in Chapter 6. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Microprocessor (schematic sheet 1)
- Address Registers (schematic sheet 2)
- Memory (schematic sheets 2 and 5)
- Memory Controller (schematic sheet 3)
- I/O Decoding (schematic sheet 4)

Microprocessor

The 8086 microprocessor (schematic sheet 1, location 10L) is used on the MPU Board to operate at a 4 MHz clock rate in the minimum mode configuration. The 8086 microprocessor outputs a 20-bit memory address. Data is accessed as 16-bit words, subdivided into a low-order byte and a high-order byte. The low-order 16 address bus lines (AD0 to AD15) are multiplexed with the 16-bit data bus. The Byte High Enable signal (BHE) is used to identify the high-order byte, while AD0 identifies the low-order byte.

Initialization or startup is accomplished with activation (HIGH) of the MPU RESET pin (location 8B) for more than four clock cycles. The 8086 microprocessor terminates operations on the high-going edge of the MPU RESET and remains dormant as long as MPU RESET is HIGH. The low-going edge of MPU RESET triggers an internal reset sequence of approximately 10 clock cycles, during which time no other operations should occur.

Non-maskable interrupt request (NMI) is initiated when external logic inputs a low-to-high transition at the NMI pin by power-up signal (PUP) at locations 11B and 11M. A non-maskable interrupt has higher priority than the maskable interrupt. A maskable interrupt is generated when external logic inputs a HIGH level at the INTR pin. The 8086 CPU responds by generating INTA for interrupt acknowledge cycle.

HOLD and HLDA are standard hold request/acknowledge signals. When external logic inputs HOLD high, the 8086 microprocessor enters a hold state upon completing the current instruction's execution; the 8086 microprocessor acknowledges the hold state by outputting HLDA high. Location 11M is the buffer for the INTR, INTA, and HLDA signals.

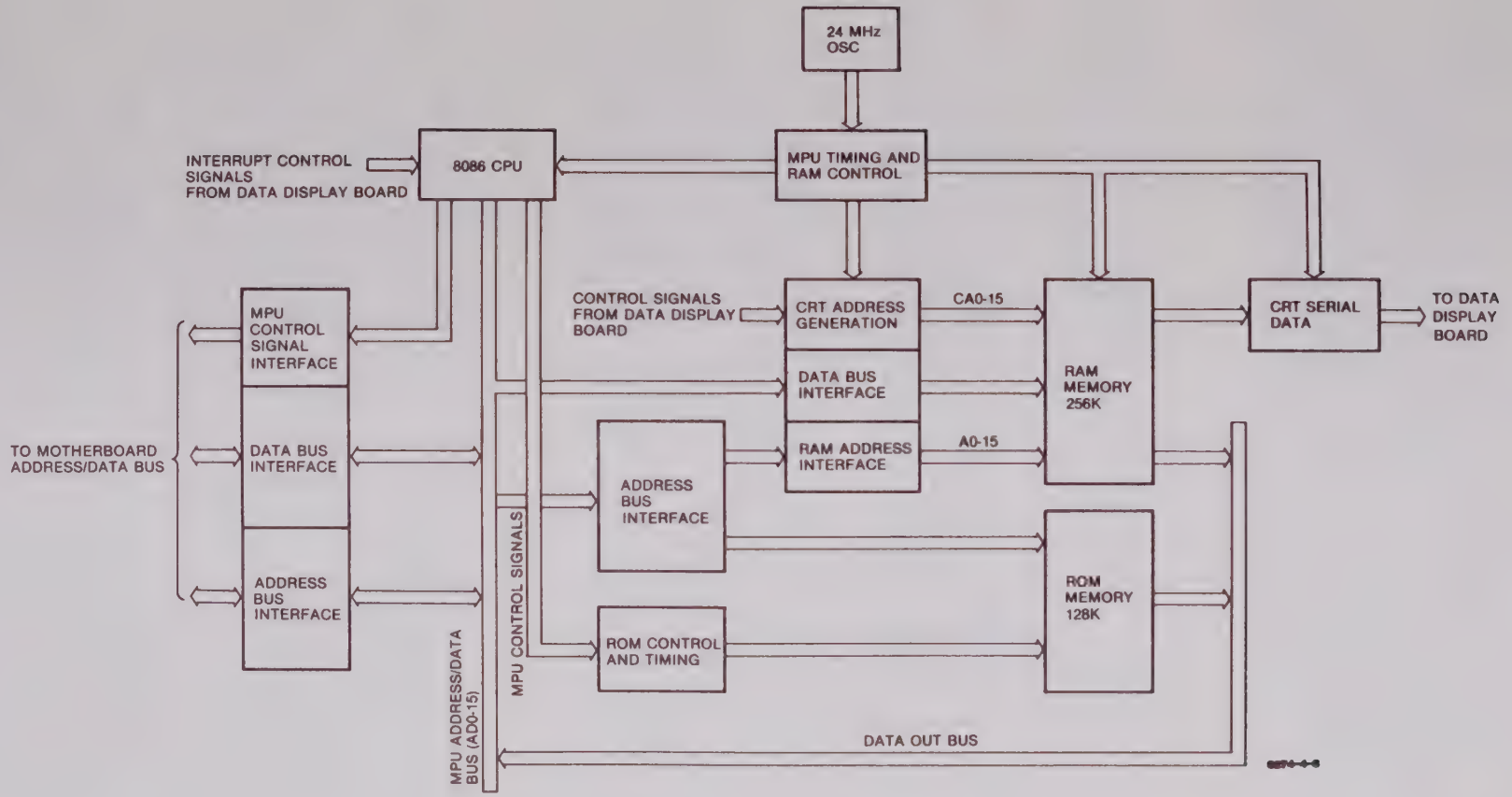


Figure 4-3. MPU Board Block Diagram

Address Registers and Data Transceivers

The 8086 microprocessor uses a multiplexed bus for address and data transfers (sheet 1 of schematic diagrams). The MPU Board demultiplexes the 8086 bus into two buses. One bus controls all information to the ROM and the RAM which is contained on locations 1A to 1H, 2A to 2H, 4A to 4H and 6A to 6H. The other bus interfaces with other boards in the K205. Locations 9K, 10K and 11K are buffers for 20 memory address lines (A0 to A19) and BHE. Locations 9M, 10M and 11L are buffers for 20 address lines and BHE to boards other than the MPU. The transceivers for the data lines are located at locations 7M and 8M. Locations 7K, 7L, 8K and 8L are wired for PROM's and buffers for temporary test only. The 8086 loads addresses into the address registers by using the Address Latch Enable signal (ALE) and then transmits (WR) the data to, or receives (RD) the data from, the address in the register.

Memory

The 8086 memory space is organized into 16 segments of 64K bytes of external memory space (sheets 2 and 5 of schematic diagrams). Segment E and F (Hex) are the 128K bytes of ROM which contains the operating software. Segment 0 - 3 (Hex) contain the 256K bytes of dynamic RAM.

The ROM segment (schematic sheet 5), locations 1A to 1H and 2A to 2H, uses sixteen 8K X 8 memories arranged into eight sections of 8K words each. Locations 3J and 3K (schematic sheet 4) are ROM chip select decoders. Data output is read from ROM through a buffer at location 3L for high-byte data and at location 3M for low byte data.

The RAM segment (schematic sheet 2), locations 3A to 3H, 4A to 4H, 5A to 5H and 6A to 6H, is made up of thirty-two 64K X 1 dynamic memories providing 128K words (256K bytes). Data is input into the RAM, through the buffer at location 4J for high-byte data and at location 6J for low-byte data via RAM WRITE DATA EN. Data output is read from RAM through the latch buffer at location 4K for high-byte data and at location 6K for low-byte data via MPU LATCH ENABLE and EN RAM READ. CRT Data is read out into buffer registers at locations 6L and 4L and then shifted out at an 8 MHz clock rate to the Data Display Board by shift registers at locations 6M and 4M.

Memory Controller

The memory timing and the clock for the 8086 microprocessor (sheet 3 of schematic diagrams) are derived from a 24 MHz oscillator (location Y1). Locations 10A, 10C, 10D, 10E, 11C, 11D, 11E and 11F are used to divide to an 8 MHz clock to the CRT and a 4 MHz clock to the 8086 clock pin. Locations 10A, 10D, 11D, 12D and 12E divide the 24 MHz clock into timing signals used to generate Row Address Strobe (RAS) at locations 10B and 8B. Additionally, column Address Strobe (CAS0 and CAS1) are also generated at locations 8A, 9A and 12C. Write Enable signals for high-byte and low-byte of both RAM segments are generated at locations 7A, 8A, 8B, 10A and 10C. Row Select, Column Select and Latch Enable for both the MPU and CRT are generated at locations 9A and 9B.

The CRT port of the memory requests a word from memory every 2 us (500 KHz). The CRT page select addresses are generated at locations 7C, 7D, 8C and 8D (sheet 4 of the schematics) by the 500 KHz clock rate from location 7B. If the 8086 requests a memory cycle during the CRT cycle, the memory controller uses the READY line on the 8086 microprocessor to generate wait states until the CRT cycle is finished and the memory can complete the requested 8086 memory cycle.

The CRT Read cycle of one word every 2 usec also provides sequential operation required for the RAM refreshing.

I/O Decoding

The MPU Board addresses other boards in the system as I/O. The PROM (schematic sheet 4) at location 10F is used to decode addresses A11 to A19. When I/O is addressed, M/IO goes LOW, causing the PROM's outputs to be HIGH. The conditions in which S.A EN is normally HIGH and DEN (Data Enable) becomes active and causes the EN OFFBOARD DATA signal at location 9C to go LOW, placing data on the bus. Read commands for RAM, ROM and S.A are generated by RD, RAM ADRS, ROM ADRS and S.A at locations 9D and 9E. Control signals RD, WR, DEN, DT/R and M/IO are also buffered out to other boards via buffers at location 9F.

THRESHOLD/GPIB/RS-232 BOARD OPERATIONS

Overview

This section describes theory of operation for the K205 Threshold/GPIB/RS-232 Board assembly, Part Number 0114-0170-30. The circuits on this board generate threshold voltage levels, convert analog voltages to digital equivalents, control the GPIB Talker/Listener interface, control the RS-232 Interface and process digital readout of external voltage input.

The Threshold/GPIB/RS-232 Board block diagram is shown in Figure 4-4. The board assembly drawing, schematic diagrams and list-of-materials are provided in Chapter 6. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Threshold Circuit (Schematic Sheet 1)
- DVM Circuit (Schematic Sheet 2)
- GPIB Interface Circuit (Schematic Sheet 3)
- RS-232 Interface Circuit (Schematic Sheet 4)
- MPU Interface (Schematic Sheet 5)

Threshold Circuit

The Threshold Circuit (sheet 1 of schematic diagram) generates four voltage sources, as follows, that may be selected for each probe: VAR A, VAR B, TTL and ECL.

The VAR A and VAR B thresholds are defined by the four 74LS273 Flip-Flop holding registers, locations 9B and 12B for VAR A, and locations 4B and 6D for VAR B. The holding registers buffer the MPU data bus to the two AD7533LN Digital-to-Analog Converters (DAC) at location 9A for VAR A and location 4A for VAR B. Separate calibration adjustments are provided for VAR A and VAR B Voltage levels. The VAR A Gain is adjusted by R6; Offset is adjusted by R9. The VAR B Gain is adjusted by R1; Offset is adjusted by R2. Both DACs have a resolution of 10 bits.

The TTL and ECL thresholds are generated by using a voltage divider network and +/- 10V reference voltage level. The calibration adjustment for TTL is R8, ECL is adjusted by R7. The +/- 10V reference adjustment is controlled by R44.

The threshold voltages are supplied as input to eight analog multiplexers (sheet 2 of schematic diagrams). The selection of a particular threshold voltage (VAR A, VAR B, TTL or ECL) used by each probe is accomplished by a set of eight analog multiplexers and eight buffer amplifiers. Six of the multiplexers, at locations 1A, 1D, 1B, 1C, 2A and 2D are tied to high and low data bytes at input sections A, B and C. Two of the multiplexers are tied to R & S latch clocks (location 2B) and J & K sample clocks (location 2C). This allows the software to select one of the four voltages as the threshold. The outputs of the analog multiplexers are buffered by the operational amplifiers (locations 1E and 2E) which provide a gain of two that increases the range of the DAC output.

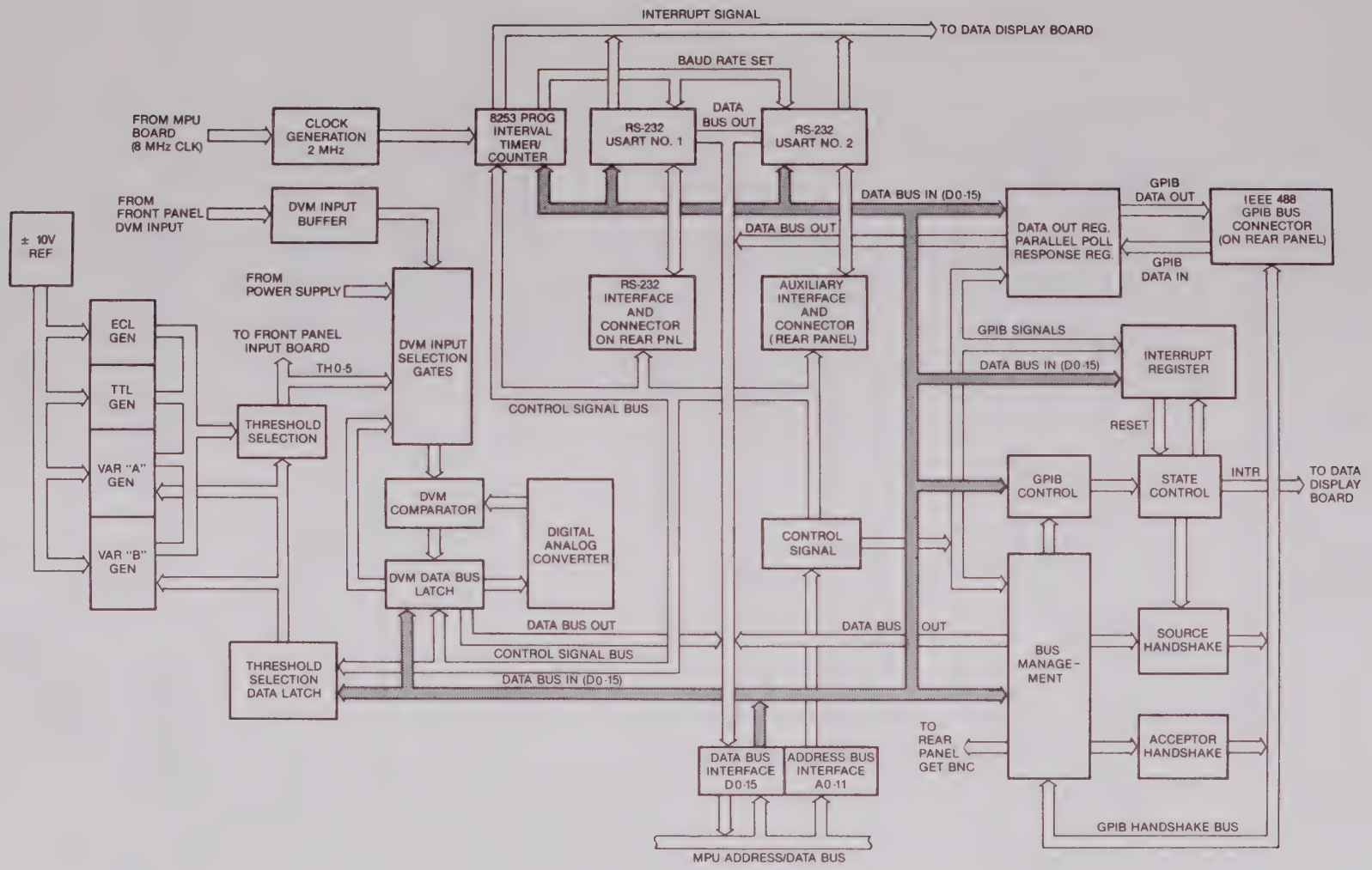


Figure 4-4. K205 Threshold/GPIB/RS-232 Board Block Diagram

One of the functions contained on the Threshold/GPIB/RS-232 Board is a software controlled Digital-to-Analog Converter and a comparator that performs Analog-to-Digital Conversions that is used by the software to check the power supply and reference voltages during power up. Three multiplexers (sheet 2 of schematic diagrams) at locations 5F, 6F and 7F are used to select any one of the power supply voltages used in the K205. The selected voltage is then scanned by the software using the 12-bit DAC at location 8A. When the DAC value exceeds the voltage being tested, the comparator (location 7A) becomes switched. The MPU compares the resulting value with a table of voltages and their tolerances to determine the pass/fail condition of the test result.

DVM Circuit

The front panel DVM input signal (sheet 2 of schematic diagrams) is buffered onto the Threshold/GPIB/RS-232 Board by the operational amplifier at location 7A and is supplied to the multiplexer at 6F. The multiplexer selects the input voltage range that is supplied to the 12-bit DAC at location 8A and the comparator. The comparator (location 7A) generates the digital value that is used by the software to specify the DVM readout.

GPIB Interface Circuit

The GPIB Interface Circuit (sheet 3 of schematic diagram) is partitioned so that the handshake required to transmit individual bytes of information (for data or control) is performed by the hardware. All message generation or interpretation is done in the software. The GPIB address and mode for Talk Only, Talk/Listen and Listen Only, are determined by the interactive display for I/O setup. Once the Mode is determined, the GPIB control register is loaded with the specified mode information and the interrupt is enabled. All I/O data transfers occur under control of the interrupt line. With Listen mode selected, the receipt of a data byte or a command at the K205 will generate the interrupt. With Talker mode selected, the interrupt is generated when the byte has been accepted by the listener I/O device.

RS-232 Interface Circuit

The RS-232 Interface Circuit (sheet 4 of schematic diagram) causes information to be entered onto the Threshold/GPIB/RS-232 Board via two 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) at locations 12D and 12E. USART #1 interfaces with the K205 back panel RS-232 port. USART #2 interfaces with the AUX port. The transmit/receive bit rates (Baud) is set by the 8253B programmable interval timer/counter at location 8E. The internal timer uses a 2 MHz clock input derived from the CPU oscillator to measure the external master clock period. The bit rate clock output supplied to the USARTS is set at 16 times the actual rate at which data is being transmitted. Plus and minus 15-volt line drivers are used to send the signals to external devices.

MPU Interface

The MPU Interface circuit (sheet 5 of schematic diagram) buffers MPU data and address lines sent to the Threshold/GPIB/RS-232 Board via the motherboard interface.

The MPU data bus (BD0-BD15) is buffered onto the board by two 74LS245 bus transceivers, locations 14F and 12F which control the two-way direction of data transfers to and from the MPU Address/Data Bus. The buffered data bytes, D0-D7 and D8-DF are transferred to, and received from on board circuits for Threshold Selection Data Latch (schematic sheet 1), DVM Data Bus Latch (schematic sheet 2), Bus Management and GET BNC output connector (schematic sheet 3), Programmable Interval Timer and RS-232 USARTs (schematic sheet 4), and GPIB Parallel Poll Register and Interrupt Register (schematic sheet 3).

The MPU address bus (BA1-BA11) is buffered onto the board by the 74LS244 Buffer/Line Drivers at locations 10F and 11F (schematic sheet 5). The jumper connector for $\overline{M}/IO$ input signal supplied to line receiver at 11F must be connected across E13 and E14 to disable the memory mapped I/O and enable the I/O mapped I/O function. The 74LS244 buffers generate three state outputs that are supplied to five 74LS138, 1 of 8 decoders, locations 9D, 10B, 10D, 11B and 11D. These decoders accept three binary inputs and output one active-low control signal (from eight possibilities) for Write Hi Byte, Write Lo Byte, Read High Byte, Read Lo Byte. The control signals are supplied to on-board circuits that control the Threshold Selection Data Latch, DVM Data Bus Latch, Bus Management circuits and rear panel GET BNC output connector, Programmable Interval Timer and RS-232 USARTS and GPIB Parallel Poll Register.

CLOCK BOARD OPERATIONS

Overview

This section describes theory of operation for the K205 Clock Board assembly, Part Number 0114-0160-10/20. The circuits on this board provide all internal clock periods and programmable logic functions. These logic functions decode external clock inputs in accordance with the Master Clock, Sample Clock and Enable Boolean Expressions selected by the instrument operator. Also, circuits for the Level Memory, which store the level at which each sample was recorded, is located on the clock board.

The Clock Board block diagram is shown in Figure 4-5. The board assembly drawing, schematic diagrams and list-of-material are provided in Chapter 6. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Internal Clocks and Probe Test (Schematic Sheets 1 and 3)
- External Clocks (Schematic Sheets 2 and 3)
- AND Master Clocks (Schematic Sheet 3)
- OR Clock Selection (Schematic Sheet 3)
- Level Memory Circuit (Schematic Sheet 4)
- MPU Interface (Schematic Sheet 5)

Internal Clocks

All Internal Clocks (sheet 1 of schematic diagram) are derived from the 100 MHz oscillator circuit containing crystal Y1. The potentiometer, R19 allows adjustment of the average value of the 100 MHz signal on the emitter of Q2 so that symmetry of the clock output at location 12C, pin 12 can be set. The variable capacitor, C8 allows adjustment of oscillator frequency.

The two 10137 BCD counters, locations 9E and 10E are connected as decade dividers to provide the 10 MHz and 1 MHz decades. The 1 MHz output of 10E goes to Q1 which shifts the level, making it compatible with the input requirements of the counter at location 9C.

The two 14518 CMOS Dual BCD Counters at locations 9C and 9D operate between -5V and ground for compatibility with the ECL level. The outputs of all six decade dividers, are supplied to inputs of the eight-to-one, 10164 multiplexer at location 10C. The MPU can select any decade as the output of 10C. For clock frequencies greater than 10 MHz, the select lines to 10C, and the 10109 OR gate at location 10D, is set to all zeros by the MPU. This enables the 100102 OR gates at location 12C to output the 100 MHz (10nsec) clock. The selected decade feeds the input to the 10016 Programmable Binary Counter at location 11B.

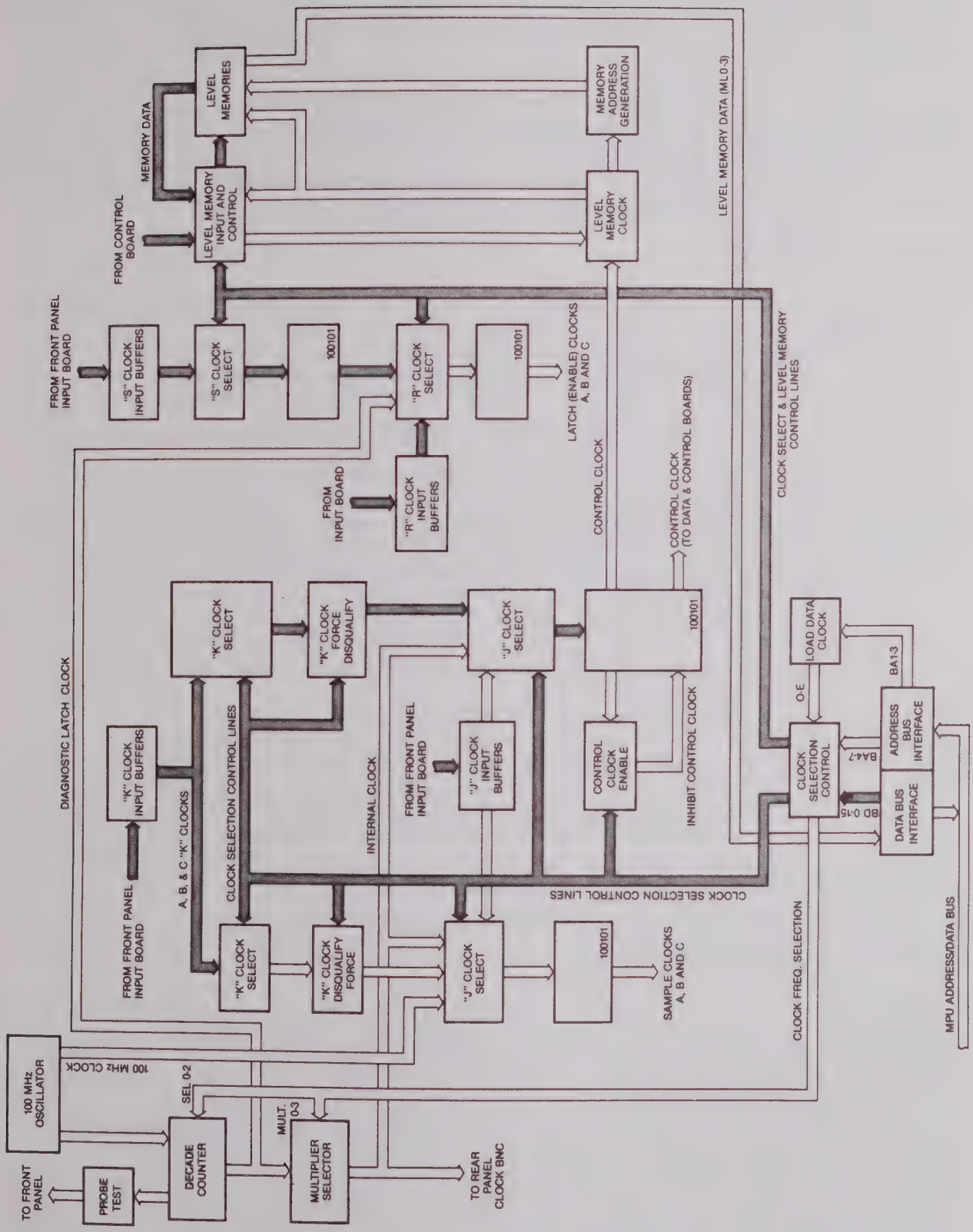


Figure 4-5. K205 Clock Board Schematic

The combination of the decade dividers combined with the programmable counter allows the selection of clock periods from 20 ns to 160 Ms in a 1 through 16 sequence. The software, however, limits the user capability to clock periods from 20 ns to 100 Ms in a 1 through 10 sequence. The BCD outputs of the 100 KHz decade counter also drives the select lines of the 4028 CMOS Demultiplexer at location 9B. The outputs of 9B provide a 1 of 8 pulse pattern to the front panel PROBE TEST connector as test data.

The 1 MHz clock and the least significant bit of BCD counter at location 9C are also supplied to the front panel PROBE TEST connector as test clocks. When an internal clock mode is selected, all external clocks are de-selected by the MPU (schematic sheet 3), and the gate at location 3H, pin 21 is pulled low, thereby enabling internal clocks to pass through to the OR gate at location 4J, pin 9.

External Clocks

The External Clocks (sheets 2 and 3 of schematic diagram) consist of seven clock circuits as follows:

- Three Latch Enable Clocks (schematic sheet 2)
- Three Sample Clocks (schematic sheet 3)
- 1 Control (Master) Clock (schematic sheet 3)

Basically, all seven clock circuits are the same. Only the Control Clock selection, which is the most complex is described in subsequent paragraphs. The Control Clock selection gates have 13 inputs as follows:

One Internal Clock

Three AND Clocks (AJ, BJ and CJ)

Three $\overline{\text{AND}}$ Clocks ($\overline{\text{AJ}}$, $\overline{\text{BJ}}$ and $\overline{\text{CJ}}$)

Three OR Clocks (AK, BK and CK)

Three $\overline{\text{OR}}$ Clocks ($\overline{\text{AK}}$, $\overline{\text{BK}}$ and $\overline{\text{CK}}$)

The major difference between Control Clock selection and the Latch Enable selection is the absence of Internal clocks for Latch Enable and the existence of Internal MPU Diagnostic Latch Enable.

AND Master Clocks Selection

The AND (Master) Clocks (sheet 3 of schematic diagram) are selected by the eight 100102 gates at locations 3H and 5H. Each of these gates has three inputs. Pin 19 is common to all gates and is driven by the output of the OR Clock selection gate at 4D. One pin of each of the 3H and 5H gates is driven by one of the J Clock inputs or their complements. The MPU controls the third input by placing a low on those gates whose J Clock input goes high when the selected clock is true. Only when all selected AND Clocks, or the OR Clock is true, will all of the outputs of 3H and 5H be low, thereby allowing the control clock at location 4J, pin 9 to go high. Synchronous start-up of the control clock is provided by the 10231 dual flip flops at location 5J. This prevents "sliver" clocks from being passed at the beginning of a record cycle.

OR Clock Selection

The OR Clocks (sheet 3 of schematic diagram) are selected by the five 100102 gates at location 5D and parts of the two gates at 4A and 4D. The MPU places a low on one input of each gate whose other input will be low when one of the selected OR Clocks is true. The OR clocks are the K Clock inputs.

Jumper selection for external clocks (schematic sheet 2, section A8) shows the jumper configuration table. With all jumpers positioned on the left two pins, the board is configured for all twelve clocks. With jumpers positioned on the right two pins, the C K Clock comes from the B S probe and the C J Clock from the B R probe.

NOTE: The software cannot read these jumpers, but instead, counts the number of Data Boards present in the system.

Level Memory Circuit

The Level Memory circuit (sheet 4 of schematic diagram) records which level of trace control is used for each word recorded on the Data Boards. Level data enters the clock board via the 20-pin header, J1.

The two 10176 registers at locations 11E and 11F and single 10173 register at location 11J operate as a pipeline which holds the level data temporarily while the decision is made to either record or not record the data. This decision is made on the Control Board which generates the Armed and Traced signals along with the level data that is sent to the pipeline. When the Traced signal is high, its complement is clocked into register 11F along with the level data. This action allows the OR gate, 12E to produce a write enable pulse on the next control clock transition. If the Traced signal is false, OR gate 12E is disabled and the level data in register 11F is written over at the next sample without being recorded. If the Armed signal goes false, the level memory becomes locked up.

The two 10016 address counters at locations 11G and 12H are used for the 10422 memories at locations 12F and 12G. The level memory is multiplexed in two ways: (1) Via the 10231 latch, pins 13 and 14 at location 11D which select the memory phase that is written to on each sample. (2) Via the 11D latch at pin 3 which provides uniform 10nsec pulses when recording is in process regardless of the sample rate.

In read mode, the OR gate at location 12D, pin 3 is disabled thereby causing the output of latch 11D, pin 3 to become 1/2 the frequency of the input. When the Armed signal goes false, the pin D input goes true thereby stopping the pulse.

MPU Interface

The MPU Interface circuit (sheet 5 of schematic diagram) interfaces the Clock Board circuits to the motherboard via edge connector P2. The 74LS85 comparator at 12J decodes four address inputs A4 through A7 from the MPU to provide the My Address signal when the Clock Board is addressed. The My Address signal enables the five 10124 TTL-to-ECL level translators at locations 6J, 7J, 8J, 9K and 10K which buffer the MPU data bus content onto the Clock Board.

The 10161 de-multiplexer at location 9J decodes address lines A1, A2 and A3 along with the MPU BWR control signal to create load pulses for the 20 10176 holding registers at locations 7A through 7H, 8A through 8H, 9G and 9H, 10J and 10H.

The 10173 multiplexer latch at location 10G multiplexes 8 bits of read data into two 4-bit nibbles which are translated from ECL to TTL levels by the 10125 translator at location 10F. The 74368 tri-state buffer at location 9F is enabled by the BRD signal sent from the MPU and the My Address signal generated by the comparator at location 12J.

The clock Board is configured with eight jumpers located at the lower left corner of the board. These jumpers select clock signals for 32-input or 48-input capability as determined by the number of Data Boards installed in the unit. When the C Option Data Board is added to an existing 32-input unit to provide 48 inputs, it is necessary to rearrange the jumper connections to enable the SECTION C clock inputs and route the B R, B S clocks into the user specified Latch Clock equation. The jumpers must be relocated from the eight center/lower-row pins to the center/upper-row pins.

NOTE: The K205 software will not recognize the SECTION C clock inputs unless these jumper connections are completed.

DATA BOARD OPERATIONS

Overview

This section describes theory of operation for the K205 Data Board assembly, part number 0114-0110-10. Each data board provides 16 inputs and either two or three identical boards may be installed in the K205 unit to provide the 32 standard or 48 extended data input configuration. The circuits on this board buffer input data signals supplied from the user's equipment, select operating modes, generate the pipeline processing functions, record traced information in main memory, decode the MPU address/data bus, and present status to the CPU.

The Data Board block diagram is shown in Figure 4-6. The board assembly drawing, schematic diagrams, and list of material are provided in Chapter 6. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Data Input Control (Schematic Sheets 3 and 7)
- Operating Modes (Schematic Sheet 3)
- Sampling Circuit Operation (Schematic Sheet 3)
- Data Pipeline Control (Schematic Sheets 2 and 3)
- Memory Control (Schematic Sheet 2)
- MPU Interface (Schematic Sheet 7)

Data Input Control

In the circuit descriptions which follow, all references are made to data input signals for AF, BF and CF which are used as an example. Circuits for the 15 remaining signals at each Input Section are identical except as noted.

The differential input signal from the probe (schematic sheet 3) is buffered onto the Data Board by the 10216 Line Receiver Buffer at location 2B (upper left corner of schematic). Output of the buffer is presented to the 10121 gates at location 2D.

Control signals from the MPU Holding Registers (schematic sheet 7) select which of the four data sources, Memory, Probe, Multiplex, or Diagnostic, will be passed through to the sampling circuitry. A description of each data source type follows:

Memory Data: This data source is a recirculation of the channel memory output which is used only for self-diagnostic purposes (Memory Select).

Probe Data: This data source is used in normal input mode (Normal Select).

Multiplex Data: This data source obtained from the low order channels is also routed to the high order channels (F-8). In this case, channel F is paired with channel 7, allowing single probing when demultiplex is selected (Demux Select).

Diagnostic Data: This data source is supplied by the MPU for self-diagnostic purposes.

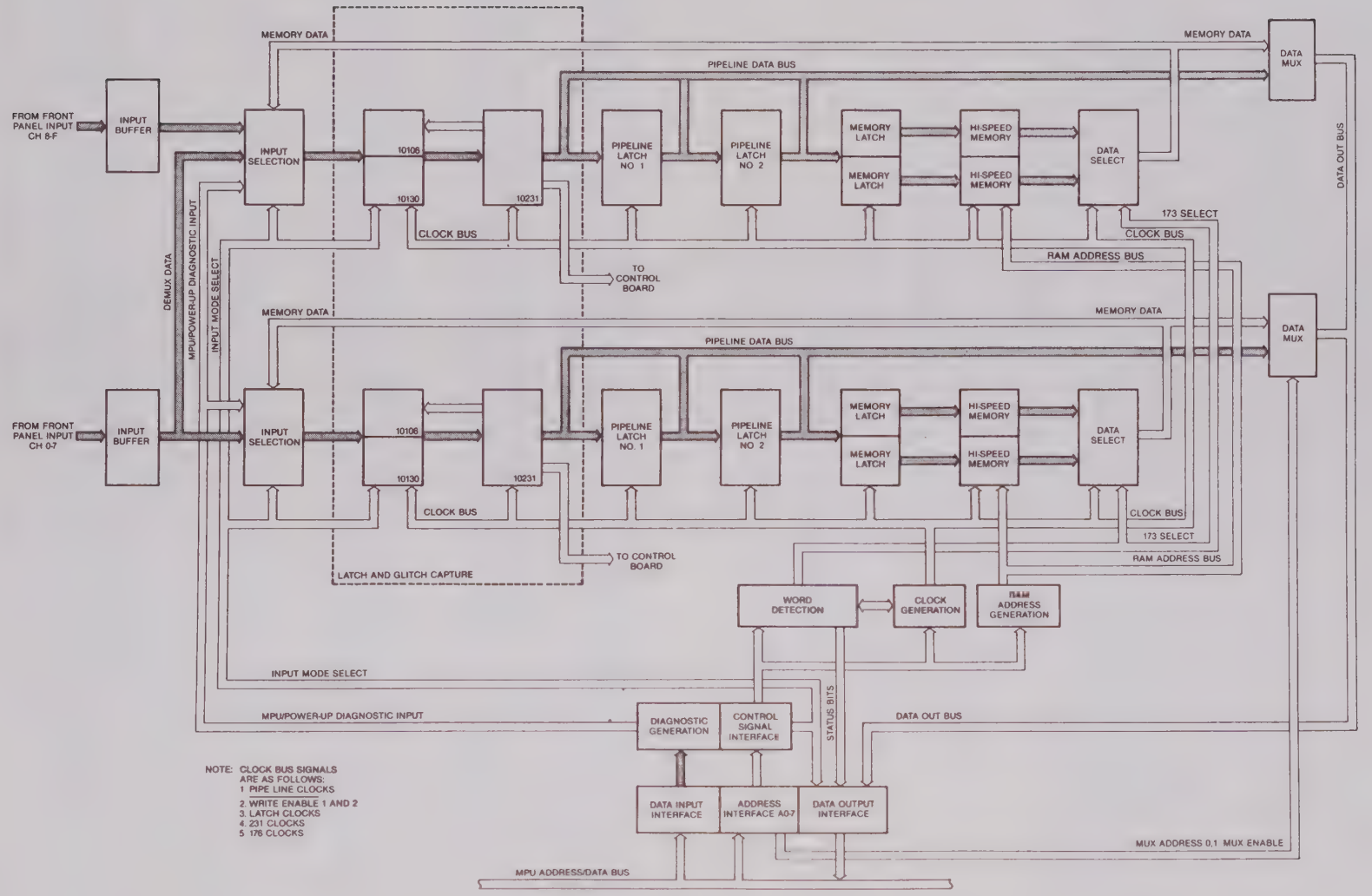


Figure 4-6. K205 Data Board, Block Diagram

Operating Modes

The output of the 10121 gate at location 2D (schematic sheet 3) is presented to the mode selection circuit consisting of two 10106 gates at location 2E, the two 10130 latches at location 2H and 10231 latches at location 2J. This circuit has three different modes of operation, Sample Mode, Latch Mode, and Glitch Mode which are described in subsequent paragraphs.

Sample Mode: Pins 6 and 12 of the 10106 gates, location 2E are held high by the MPU, causing these gates to become disabled in sample mode. Pins 6 and 9 at the 10130 latch, location 2H are held low by the MPU which causes the latch output to follow the input asynchronously. The 10231 latch at location 2J is the sample register. The input data is transferred to the output and held at the rising edge of the sample clock on pin 9.

Latch Mode: The gate, 2E is disabled as described in Sample Mode. Pin 6 of the 10130 latch at location 2H is held low allowing the Latch Enable Clock at 2H, pin 9 to control the latch. When the latch clock is low, 2H is transparent as in sample mode. When the latch clock goes high, the data that was true at the clock transition is held at the output. The 10231 sample register at location 2J functions the same as sample mode conditions.

Glitch Mode: The MPU signal Glitch Disable, is low in this mode allowing outputs of the 10106, location 2E to be controlled by the input data and the data in the sample register. The MPU signal, Glitch Enable, is high in this mode, thereby disabling the D input pin of the 10130 latch at location 2E. The state of the 2H latch output is then controlled by the outputs of 2E via the asynchronous set and reset pins.

Sampling Circuit Operation

The sampling circuit (sheet 3 of schematic diagram) operates as follows: Assume that pin 2 of the 10130 and 10231 latches, at locations 2H and 2J respectively, are high at the start of operation. The input pin 5 of gate 2E is high thereby disabling the upper gate that goes to pin 5 of latch 2H. The input at pin 13 of gate 2E is low which allows any low input signal to reset 2H, pin 2 by placing a high on the direct reset, pin 4. Pin 2 of latch 2H remains in this new state regardless of any activity on the input signal. At the next sample clock, the output of pin 15 at latch 2J goes low which enables the upper gate of 2E to respond to a high input signal only. If the input signal goes high at anytime, the signal at pin 3 of gate 2D goes low causing pin 3 of gate 2E to go high which sets the output of latch 2H to a high condition for the next sample clock. In addition to going to the Glitch Feedback Comparison Gates, outputs of the register are also supplied to: (1) the 10174 multiplexer at location 2L for MPU diagnostic access, (2) the pipeline register 10176, location 2K, and (3) inverted data from pin 14 of latch 10231 goes to the Control Board word recognition circuits.

Data Pipeline Control

The Data Pipeline (sheet 3 of schematic diagram) consists of two stages of D registers contained in the 10176 latch at location 2K. The source of the pipeline clock depends on either of two clock modes selected as follows: In most modes, the pipe clock is the same as the Master (Control) Clock. In Store mode, the pipe clock is the same as the sample clock.
Note that the data in both stages of the pipeline is also present at the 10174 multiplexers, locations 1L and 2L for diagnostic access.

Pipeline data is also presented to the inputs of both 10176 registers at locations 6D and 6E which begin two-way memory multiplexing. The registers at locations 6D and 6E act as pre-memories and are clocked by the rising edge of signals $\overline{WE}$01 and $\overline{WE}$02 respectively, which are output from the OR gates, location 6J or schematic sheet 2. The $\overline{WE}$01 and $\overline{WE}$02 signals are 180 degrees out of phase, which causes samples to be stored alternately in the two 10422, 256x4 RAMs at locations 5B and 5C. The 10173 demultiplexer at location 5D demultiplexes the memory. The data out of 5D goes back to the 10121 input selectors at location 2D for diagnostic recirculation and to the multiplexers at location 1L and 2L for MPU access.

Memory Control

The Memory Control logic (sheet 2 of schematic diagram) is implemented by the 100155 Mux Latch at location 6H which keeps track of control signals from the MPU and Control Board. This Mux Latch also controls which phase of memory will be written to, or read from, next via the 01 and 02 signals which alternately enable the two 100101 gates at location 5J.

When Internal Clock is used, the OLD TRACED signal, output from pin 2 of 6H combines with the $\overline{\text{ASYNCH MODE}}$ signal from the MPU to form the $\overline{\text{MEMORY ALIVE}}$ signal which enables pins 5 and 9 of the 100101 gates at location 5J.

When External Sample Clocks are selected, the $\overline{\text{MEMORY ALIVE}}$ signal is derived from the $\overline{\text{SYNC MODE}}$ MPU control signal and the $\overline{\text{TRACED}}$ signal from the Control Board. The outputs of pins 5 and 9 at location 5J are the $\overline{WE}$ pulses for the record memories.

The HALTED output signal from Mux Latch at location 6H disables the OR gates at location 5K. These gates pass the sample clock and select the source of the pipe clock. The OR gates at location 6J distribute all clocks and the $\overline{WE}$ signals. Note that the width of 173 clocks at gate 6J, pin 13 is set by a difference in propogation delay when the same signal feeds both inputs via two different paths.

MPU Interface

The MPU Interface circuits (sheet 7 of schematic diagram) decode the MPU Address Bus via the 10124 TTL to ECL Translator at location 8K, the 74S85 four-bit comparator at location 9M and the associated circuits. The 10124 translators at locations 6M, 7L, 10L and 9K are also used as TTL to ECL level translators for the data bus. These translators feed the inputs of the 10176 Hex D Latches which hold control information from the MPU.

The 10173 Multiplexers at locations 12M and 13M multiplex the lower 8 bits of Read data to the MPU. The 10125 TTL to ECL level translators at locations 1M, 2M, 3M and 11M translate TTL logic levels received from the bus to ECL logic level for data board interface.

CONTROL BOARD OPERATIONS

Overview

This section describes theory of operation for the K205 Control Board assembly, part number 0114-0120-10. The Control Board contains all decision making logic for controlling the recording process. This includes word recognition circuits, delay counters, and the logic to combine delay conditions with detected words. These circuit functions cause the K205 unit to stop recording, jump or advance to another level with different record parameters and selectively enable or disable the recording operation.

The Control Board block diagram is shown in Figure 4-7. The board assembly drawing, schematic diagrams, and list of material are provided in Chapter 6. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Word Recognition Circuits (Schematic Sheets 1, 2, and 3)
- Word Selection Circuits (Schematic Sheets 4 and 5)
- Level Switching Circuit (Schematic Sheet 6)
- Delay Counter (Schematic Sheet 8)
- Recording Control Circuits (Schematic Sheet 7)
- MPU Interface (Schematic Sheet 9)

Word Recognition Circuits

The Word Recognition Circuits are contained on sheets 1, 2 and 3 of schematic diagrams. Word recognition is accomplished separately for each Input Section, A, B, and C with the separate words being combined in the word selection circuits described in subsequent paragraphs. In the circuit descriptions which follow, all references are made to the Section C Input (schematic sheet 3) which is used as an example. Sections A and B operate identically to Section C.

The $\overline{DATA}$ signal supplied from the $\overline{Q}$ output of the sample registers on the C Data Board enters the Control Board via the motherboard and is synchronized with the control clock in the 10176 registers at locations 1H, 2H, and 3H. The data output from these registers is presented to four of the eight address inputs, and to each of the four 10422, 256x4 Static RAMs at locations 1G, 1F, 3G and 3F. The other four address lines of the RAMs are driven by the LEVEL X signal, where X is the 4-bit number representing the level of trace control. The four data outputs of the 10422 RAMs correspond to the four combinational functions of the K205 for STOP, JUMP, ADVANCE and TRACE signals generated by the 100101 OR gates at locations 1D and 3D.

The MPU initializes the RAMs to contain zeros only at those address locations and bit positions that correspond to the combinations selected by the user for STOP, JUMP, ADVANCE and TRACE at each level.

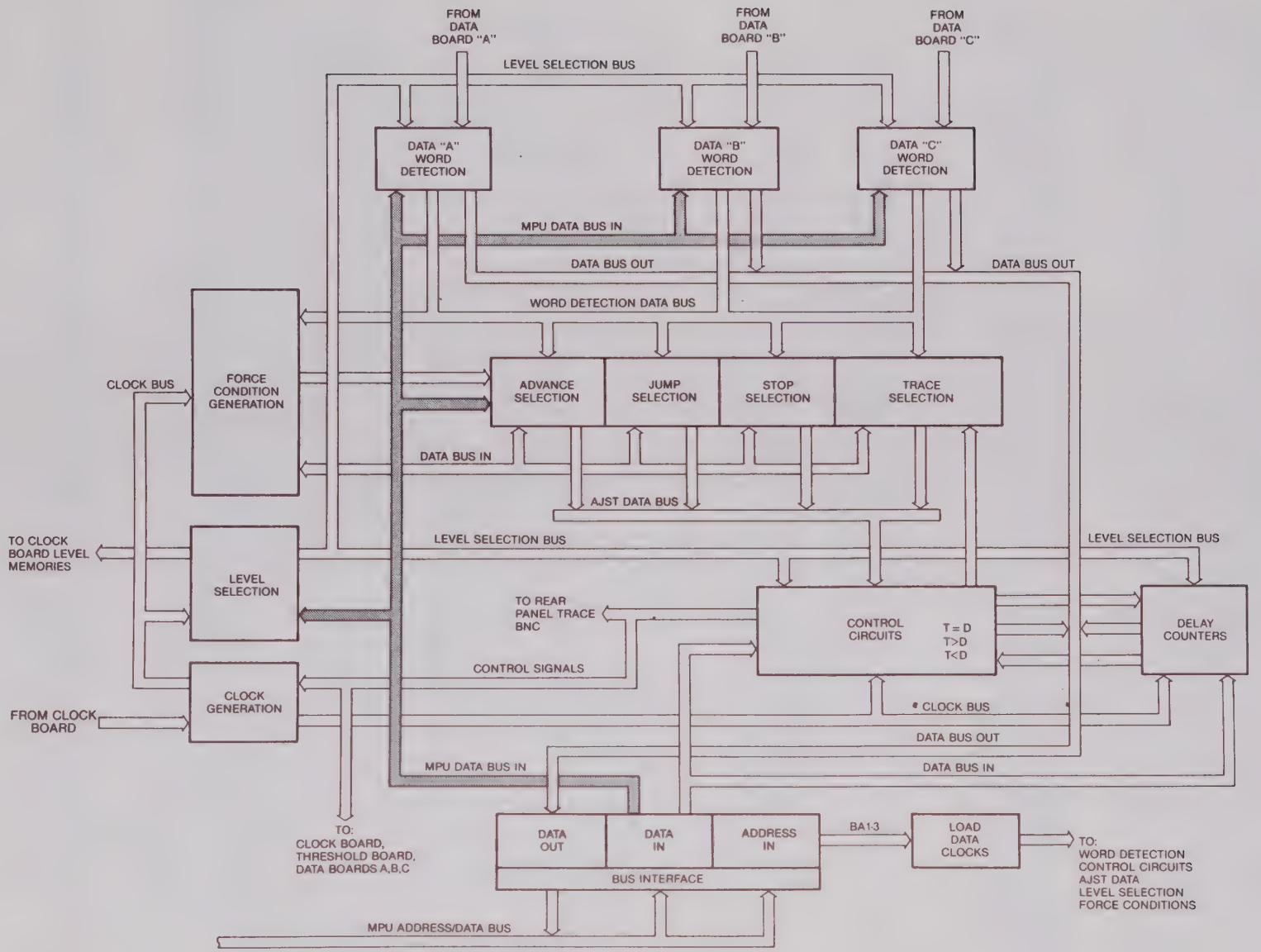


Figure 4-7. K205 Control Board Block Diagram

The RAMs therefore function as programmable logic arrays which respond to different STOP, JUMP, ADVANCE and TRACE combinations at each of 16 levels for a total of 48 combinations. The 100101 OR gate at 3D combines the outputs from four RAMs into the signals for STOP C, JUMP C, ADVANCE C and TRACE C (where C = Section C Inputs). The 10176 Holding Register at location 2J stores MPU control signals that are used during initialization. The 10164 Multiplexer at location 4C gives the MPU access to section outputs for diagnostic purposes.

Word Selection Circuits

The Word Selection Circuits are found on Sheets 4 and 5 of the schematic diagrams. The signals for STOP A, B, and C; JUMP A,B,and C; ADVANCE A, B, and C, and TRACE A, B, and C are combined with the delay condition signals $\overline{T<D}$, $\overline{T=D}$ and $\overline{T>D}$ in these circuits. For purpose of this discussion, only the ADVANCE select circuit will be considered. The STOP, JUMP and TRACE circuits generally operate in the same manner as the ADVANCE circuit.

The signals for ADVANCE A, B, and C, and their complements along with the delay condition signals $\overline{T<D}$, $\overline{T=D}$, and $\overline{T>D}$ are presented to the inputs of the 100102 gates at locations 5C and 5D. Each of these gates is also supplied with one of the outputs of the 10145A High Speed, 4x16 RAMs at location 4B, 5B and 6B. The outputs of gates 5C and 5D are NORed together in the 100101 gate at location 5F whose input must be low for the ADVANCE signal to go high. The ADVANCE signal will be low if any of the gates at location 5C or 5D have lows on all three inputs. Pin 19 of gates at locations 5C and 5D is common to all gates and is low at all times except during Diagnostic Tests or when the Arm Initialization condition is present and the MPU can pull it high for the FORCE ADVANCE condition, as presented in the following example operation.

1. Assume the user has selected conditions for:
   Advance if Data=A and T=D

2. For this selection, the MPU would initialize the 10145A High Speed RAMs to place a low state at pins 1 and 17 of gate 5C. Signals at the appropriate level would be applied to pins 17 and 24 of gate 5D.

3. The controlling input signals to these gates become: ADVANCE B, $\overline{T<D}$, $\overline{T>D}$, ADVANCE C, and ADVANCE A.

4. If any one of these signals is low, indicating the selected equation is false, the output of the gate it controls will be high, causing $\overline{\text{ADVANCE}}$ to be true and ADVANCE to be false.

The address inputs to the 10145A High Speed RAMs is the 4-bit LEVEL number (e.g., LEVEL 3C, LEVEL 2C, LEVEL 1C and LEVEL 0C). It is therefore possible to select a different Advance equation for each of the 16 levels of trace.

The inputs to the 100101 OR Gate at location 7D parallel the inputs supplied to OR Gate at location 5F which are controlled by the Word Recognition Logic, disregarding the delay conditions. The outputs of 7D are called EVENT and $\overline{\text{EVENT}}$ which are used to control the delay counter in Events Delay Mode.

The 10176 Registers at locations 6A and 7A are used to hold MPU control signals which can force the signals for STOP, $\overline{\text{STOP}}$, JUMP, $\overline{\text{JUMP}}$, ADVANCE, $\overline{\text{ADVANCE}}$, TRACE, $\overline{\text{TRACE}}$, EVENT, and $\overline{\text{EVENT}}$ to a desired logical state by overriding the normal input conditions. These signals are used during the Diagnostic Checks and the Arm Initialization Sequence.

The register at 6A also enables the 10231 Latch at location 5A to FORCE ADVANCE for one clock period. This is used for manual advance and to begin the armed cycle when the unit advances from Level F into Level 0 on the first control clock.

Level Switching Circuit

The Level Switching Circuit is contained on sheet 6 of the schematic diagrams. The 100155 IC at location 5G is a Quad Multiplex Latch. The two sets of inputs to the latch come from the two 10145A RAMs at locations 5H and 5J. The address input to 5H and 5J is the 4-bit number level. The 5H and 5J RAMs are initialized by the MPU so that for any given level address, 5H contains the number of the user selected Jump To Level.

The 100155 has two Enable inputs, both of which must be in a low state for the selected input to be transferred to the output as the next level. One of the Enables is driven with the $\overline{\text{JUMP OR ADVANCE}}$ control signal, allowing the level to change only when a JUMP or ADVANCE condition is detected. The other Enable is a 3nsec pulse derived from the control (master) clock. The new level then becomes the new address for the Level RAMs 5H and 5J. The propagation delays around the loops are that much greater than the 3nsec Latch Enable pulse that allows glitch-free operation to occur. The $\overline{\text{JUMP}}$ condition present at pins 16 and 17 of 5G selects which set of inputs will become latched. Therefore, the decision to jump or advance gives priority to jumping even when the advance condition is true at the same time.

Delay Counter

The Delay Counter circuit is shown on sheet 8 of the schematic diagrams. The 10016 at location 13C and 13E form a simple Programmable Synchronous Counter. The 10145 RAMs at location 14C and 14F are addressed by the Level. Each address is initialized by the MPU with the two's complement plus 1 of the delay number for the corresponding Level.

Recording Control Circuits

The Recording Control circuits are shown on sheet 7 of schematic diagrams. The ICs at location 12A, 12B and 14B store the status of the Control Board that was present prior to the most recent transition of the control clock. Note that all output signal names are expressed in past tense. The input conditions that caused the outputs to become true may not always remain true after being latched. These remembered state signals are decoded by gate circuits located at 11D, 11C, 11B, 11A, 11F and 9B along with the DELAY TOP COUNT (TC) signal (supplied from location 11D on sheet 8 of schematic). The TC signal controls the delay status bits, T=D, T<D, and T>D to stop recording at the correct time and to control the process of selective trace recording.

The 100155 Mux Latch at location 12B has three inputs, $\overline{\text{EVENT}}$, $\overline{\text{ADVANCE}}$ and JUMP. Two of these inputs $\overline{\text{ADVANCE}}$ and JUMP are connected to both the A and B Mux inputs and are clocked to the output regardless of the state of the Mux Selection Control on pins 16 and 17 of 12B. The two output signals ADVANCED and JUMPED are ORed together at location 11C, to form the $\overline{\text{DELAY PE}}$ signal, which allows the delay counter to become loaded on the next clock transition and Advanced or Jumped which is used to control the states of the delay condition signals.

The Mux Select control signal for 12B is the EVENT MODE signal which is output of the 10145A RAM at location 13A. This bit is high at those levels in which the user has selected Events Delay Mode. If EVENT MODE is low, the A Mux inputs of 12B are selected causing output pin 9 of 12B to become latched low only when $\overline{\text{EVENT}}$ is low.

The output signal at pin 9 of 12B is called $\overline{\text{EVENTED}}$ and is combined with the $\overline{\text{OLD T=D}}$ signal (which is at a low state if T was less than D prior to the last clock) to form the $\overline{\text{DELAY CE}}$ signal. Therefore, operation in Events Delay Mode only allows the Delay Counter to increment once for each sample on which the selected event combination was true.

The 10055 Mux Latch at location 14B also has three inputs, ADVANCE, STOP and TRACE. The STOP and TRACE inputs are connected to both the A and B Mux inputs. The STOP input signal becomes STOPPED after being clocked through 14B and causes the ARMED signal to become false thereby ending the recording process. The TRACE input signal becomes TRACED and $\overline{\text{TRACED}}$ after being clocked. The TRACED signal is combined with ARMED and is fed to a BNC connector on the rear of the K205 chassis as the TRACE signal. The $\overline{\text{TRACED}}$ signal is routed to the Data Boards where it is combined with the ARMED signal to allow the sample that caused the trace condition to be recorded.

The third input to Mux Latch at location 14B is the ADVANCE signal which is connected only to the B Mux input at pin 15. The Mux control input which determines whether ADVANCE will be latched in 14B is the END LEVEL signal which is one of the outputs supplied from the 10145A RAMs at location 13A. The END LEVEL signal will be high only at Level F.

The output signal at pin 9 of 14B is called ADVANCED and ENDED. As the name implies, the signal will be true only if Advance and End Level are both true when 14B is clocked. The Advanced and Ended condition causes the ARMED signal to go false thereby ending the recording process.

The 10176 Mux Latch at location 12A has six inputs: $\overline{\text{D=1 IF JUMP}}$, $\overline{\text{D=1 IF ADVANCE}}$, CYCLE RESET, $\overline{\text{T<D}}$, $\overline{\text{T=D}}$, AND $\overline{\text{T>D}}$. The CYCLE RESET signal is used only by the MPU during the Arm Initialization cycle or during Self Diagnosis. The other five inputs to 12A coordinate the switching of the delay status bits. The signals for $\overline{\text{D=1 IF JUMP}}$ and $\overline{\text{D=1 IF ADVANCE}}$ are supplied from the 10145A RAM at location 13A. These signals provide a look ahead function to provide delays of one which the 10016 Delay Counter cannot provide. The signals for $\overline{\text{D=1 IF JUMP}}$ and $\overline{\text{D=1 IF ADVANCE}}$ will be low only if the next level (either the JUMP-TO or ADVANCE-TO level, or both) has a delay of one selected.

The outputs of 12A for $\overline{\text{D=1 IF JUMPED}}$ and $\overline{\text{D=1 IF ADVANCED}}$ are combined with the $\overline{\text{JUMPED}}$ and $\overline{\text{ADVANCED}}$ signals respectively at location 11C and 11D to cause the T=D signal to become true immediately upon entering a level with a delay of one selected.

The signals for $\overline{\text{T<D}}$, $\overline{\text{T=D}}$ and $\overline{\text{T>D}}$ are clocked through 12A to become $\overline{\text{OLD T<D}}$, $\overline{\text{OLD T=D}}$ and $\overline{\text{OLD T>D}}$. These three signals also must be present at 11B, 11C, and 11D to ensure proper cycling of the delay condition bits. The 10164 Multiplexers at locations 12C and 12F provide access for the MPU to determine record control status for self-diagnostics.

MPU Interface

The MPU Interface is shown on sheet 9 of the schematic diagram. The 74LS85 Comparator at location 13H decodes the address bus to enable the interface only when the Control Board is addressed. The 10124 Translators at locations 11H, 8J, 7J, 3J and 10H provide TTL to ECL level translation for the 16 line address/data bus. The read data from the Control Board is multiplexed down to only four lines. These lines are translated from ECL to TTL levels by the 74368A Three-State Inverter Buffer at location 12H. The 10161 Demultiplexer at location 13G decodes Address Lines A1, A2 and A3 along with the $\overline{WR}$ signal from the MPU to provide LOAD signals for the MPU programmable holding registers, word detection RAMs and control RAMs.

Chapter 5

DISK DIAGNOSTICS

INTRODUCTION

This chapter provides the technician with descriptions of, and instructions for executing diagnostic test routines contained on the K205 Master Diagnostic Disk, Gould part number 0120-0167-10. Separate test routines are provided for each printed circuit board and associated circuits, excepting the MPU Board. The MPU Board is tested by the K205 Power-Up diagnostic firmware which verifies the operational status of the MPU Board whenever the K205 unit is initialized. The MPU Board must therefore be functional to load and execute the K205 Disk Diagnostic Routines.

The K205 Diagnostic Operating System (DIAG) software is organized as shown in Figure 5-1. The operating system is a monitor control program designed to checkout hardware/software functions for K205 printed circuit boards and components. The K205 DIAG is driven by the 8086 CPU on the MPU Board. the diagnostic routines are executed by using keys on the keyboard to select and set up a specific test module and control the testing operating.

Major features of DAIG are as follows:

- DIAG provides a menu for the operator to enter options and parameters. The individual Diagnostic modules use these options to determine program flow and operation.

  These options specify which boards in the system are to be tested, the number of times to repeat each test, halt diagnostic execution upon error, loop diagnostic execution upon error, test floppy disk Drive A or B, test Drive Side 0 or Side 1, display or suppress error messages and allow operator interaction while running the Diagnostics. These options and parameters are explained in a later section.

- DIAG loads Diagnostic modules from Disk and executes them. The Diagnostic modules consist of six programs on the K205-D disk and are loaded in one at a time, and executed. Due to the size of the modules, (up to 40k in length), and the limited RAM space available, (64k), it would be impossible for all of the code required to test the K205 to be resident in memory at once.
  So when DIAG is testing a particular board, the appropriate Diagnostic module is then loaded in from the Disk as an overlay and executed. These Diagnostic modules are discussed in a later section.

- DIAG provides Pass/Fail History information.
  DIAG keeps a tabulation of each time a test is executed, and whether it Passed or Failed. This information is accumulative, so if the Diagnostic is run for a long period of time, the Pass/Error information is a total representation of all Passes and Errors.

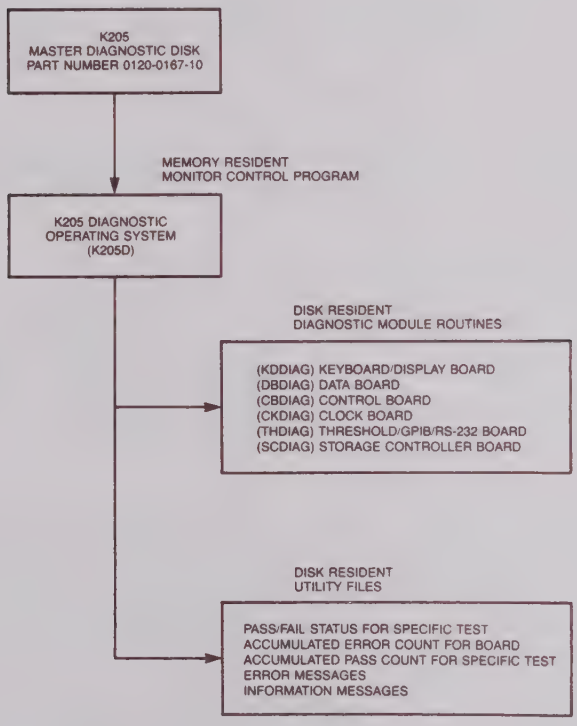


Figure 5-1. Organization of K205 Diagnostic Software

NOTE: The maximum number of Passes and Errors DIAG can log is 65,535. If the error count reaches this limit, it will not wrap around to 0, rather DIAG will stop incrementing this count.

STARTING UP THE K205 DIAGNOSTICS

```
* * * * * * * * * * * *CAUTION* * * * * * * * * * * * * *
*                                                       *
*    Prior to using the K205 Master Diagnostic          *
*    Disk, it is recommended that the user format       *
*    and copy the master disk as described in the       *
*    K205 Disk Storage System User's Manual Addendum.   *
*    Store the master disk and use the duplicate as     *
*    a backup to avoid possible damage to the original. *
*    Ensure the duplicate disk is write protected to    *
*    prevent inadvertent writing that could destroy     *
*    data.                                              *
* * * * * * * * * * * * * * * * * * * * * * * * * * * * *
```

When The K205 Logic Analyzer is powered on, it will perform it's power on self test Diagnostics. Assuming these have Passed, the Logic Analyzers's default menu will be displayed. To boot up the Disk Operating System, insert the mini Floppy Diskette into Disk Drive A with the Write protect tab nearest to the activity light, and close the door on the Drive. Press the "I/O" key, then press "1". This will "boot up" the Disk Operating System and the screen display should change to show the directory contents of the Diskette. The following files should be in the display:

K205D -01.EXE	(K205 Diagnostic Operating System)
KDDIAG-00.EXE	(Keyboard/Display Diagnostic Module)
DBDIAG-00.EXE	(Data Board Diagnostic Module)
CBDIAG-00.EXE	(Control Board Diagnostic Module)
CKDIAG-00.EXE	(Clock Board Diagnostic Module)
THDIAG-00.EXE	(Threshold/GPIB Board Diagnostic Module)
SCDIAG-00.EXE	(Storage Controller Diagnostic Module)

Other files may be listed, but they are irrelevant to the Diagnostics.

The diagnostic modules for KDDIAG, DBDIAG, CBDIAG, CKDIAG, THDIAG and SCDIAG are not executable as stand alone programs. They are loaded in and executed by K205D-01.EXE. If a "RECALL" is done on one of these modules, the K205 will lock up, and the power will have to be turned off, and restored to reset system operations.

To load the K205 Diagnostic, press the NEXT key until the DOS "RECALL" selection appears. Press the right arrow key to enter the filename field. Press the down arrow key until K205D-01.EXE is highlighted. Press the F4 key. This loads DIAG from the Disk and executes it. The K205 Diagnostic Main Menu is then displayed.

DIAG MENUS AND DISPLAYS

Main Menu

The "main" menu is displayed upon booting up DIAG. This main menu has three main fields as follows:

The top of the screen has a list of the keys, and a description of the function for each key. Throughout the Diagnostic execution, the top of the screen will have a list of keys. The keys listed and the functions of these keys will vary, depending on the particular state or menu the Diagnostic is in.

The lower-right side of the screen has a list of the "Active" boards in the system. When DIAG began executing, it determined which boards were installed in the K205 chassis. The boards that it found are designated as "Active", and these are the boards that are tested.

The lower-left side of the screen has a list of the "Inactive" boards, or the boards that are not present in the system. Some boards are optional, and since DIAG was written to test all possible components of a K205 system, boards that are not present are displayed as "Inactive", indicating that these boards will not be tested.

NOTE: The "Active" and "Inactive" status can be forced or overridden. If, for example, a board is actually present in the system, but you do not wish it to be tested, you can force it to become Inactive by positioning the cursor with the up or down arrow keys, next to the name of the board, and press the left arrow key. This action will place the board into Inactive status. This can be done for any or all boards.

Boards that are flagged as "Inactive" can be forced to become "Active" by positioning the cursor using the up or down arrow key, next to the name of the board and pressing the right arror key. This would be useful if a board is actually in the system but is faulty, and caused it to appear in the "Inactive" status when DIAG started up. The board can be forced "Active" and tested.

Of course if a board is not in the system, and it is forced to be "Active" and the Diagnostic is run, it will Fail and give you non relevant information.

System Testing (All Active Boards)

When DIAG is started and the Main Menu is displayed, the Active/Inactive/Test >>> cursor will be pointing to "All Active Boards". If the NEXT Key is pressed, all of the tests for all of the boards in the "Active" list will be automatically tested sequentially.

Before each test is executed it will be loaded in by DIAG and the message "Loading Diagnostic File" will be displayed. The name of the current Diagnostic module will be displayed at the top and the test names and test steps will be updated.

During this automatic testing DIAG will display the number of Passes and Errors at the bottom of the screen. If there are any Errors, an Error message will be displayed at the center of the screen, and the Error count at the bottom of the screen will be incremented. The Pass counter at the bottom of the screen will not be incremented until all tests for all Active boards are performed.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key will abort the current test and return to the Main Menu.

System Testing is normally performed if an overall picture of the unit's integrity is desired. Since all Subtests for all Active boards will be performed, this testing will take quite a while.

Single Board Testing

If a single board is to be tested, the Test >>> cursor should be positioned next to the name of the board and the NEXT key pressed. This method is different from testing "All Active Boards" in several ways as follows:

First,the testing is performed only on the chosen board.

Second, the testing is not started automatically. The Subtest Menu list for that particular Board will be displayed, and either all Subtests can be executed, or a single Subtest can be executed.

Third, the Pass and Error count is not displayed at the bottom of the screen.

Single Board testing is done when the integrity of a single board or boards is unknown, and a direct test on the board in question is performed. This method provides information at a quicker rate than if all the previous boards in the Active list are tested.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key will abort the current Subtest and return to the Subtest Menu.

Conducting All Subtests or Individual Subtests

When a single board is selected for testing, the Subtest Menu is displayed. A single Subtest can be performed by positioning the highlighting cursor, using the up or down arrow keys, over the desired test and pressing the NEXT key. The single Subtest will run, and then return to the Subtest Menu. If the parameter selection for NUMBER TO REPEAT TESTS is greater than 1, the particular Subtest will be repeated that number of times.

Selecting "ALL SUBTESTS" executes all of the tests in the Menu sequentially, and returns to the Subtest Menu when complete.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key will abort the current Subtest and return to the Subtest Menu.

Pressing the PREVIOUS key restores the Main Menu.

DIAGNOSTIC PARAMETERS (EDIT KEY)

General

There are a number of options or parameters available for execution of the Diagnostic modules. These parameters control the program flow of execution. The parameters can be displayed and/or changed at any time by pressing the EDIT key. This will display the list of parameters, and the current selections.

Once the parameter options are selected, pressing the PREVIOUS key will return you to the previous Menu Display or program execution.
The parameters are changed by positioning the highlighting cursor next to the desired parameter and pressing the NEXT key. This will select the opposite of the currently displayed option, i.e. YES changes to NO. This method is valid for all parameters except the Times to Repeat Test, which is explained later.

The parameters are as follows:

Parameter	Options	
1. Halt on Error	No, Yes	(default is No)
2. Loop on Error	No, Yes	(default is No)
3. Display Error Messages	Yes, No	(default is Yes)
4. Times to Repeat Test(s)	1 - 65535	(default is 1)
5. Test Floppy Disk Drive A	No, Yes	(default is No)
6. Test Floppy Disk Drive B	Yes, No	(default is Yes)
7. Test Side 0 of Drive(s)	Yes, No	(default is Yes)
8. Test Side 1 of Drive(s)	Yes, No	(default is Yes)
9. Run Operator Action Tests	No, Yes	(default is No)

Halt on Error

The first parameter, Halt on Error, specifies that if an Error occurs during execution of the Diagnostic, the Diagnostic will temporarily halt and the Error message remains on the screen. A "HALTED ON ERROR" blinks on the screen to verify that the Diagnostic is halted. Diagnostic execution can be resumed by depressing the NEXT key. If another error occurs, DIAG again halts until the NEXT key is depressed.

Normally when there is an Error, and the Halt on Error parameter is not selected, the Error message is displayed on the screen for about a second. This doesn't allow adequate time to read all of the information displayed, so Halt on Error is useful for "single stepping" through the Errors that occur.

The disadvantage of Halt on Error is that when an Error occurs, all testing is suspended, and the NEXT key must be entered to resume. In the case where you want a unit to run the Diagnostics for a period of time without the need of operator actions, and then later check on the number of Passes and Errors, Halt on Error should be disabled by setting the option to "NO".

Loop on Error

Loop on Error specifies that if during the execution of the Diagnostic an Error occurs, the Diagnostic will loop on the test step that found an Error. This test step will be repeated continuously even if it occasionally Passes.

The Loop on Error option is useful for debugging a board. If for example, a board is intermittently failing, the continuous looping allows the operator to trigger on a Write pulse, a Read pulse or a Clock.

The looping continues until either the CONTROL key is pressed, or the Loop on Error option is disabled by pressing the EDIT key, and changing the selection to "NO".

NOTE 1: The CONTROL key is used during the process of Looping on Error. Pressing the CONTROL key "skips" out of the current Test Step and proceeds to the next Test Step. It provides a means to quickly abort a Test Step without changing the Loop on Error Parameter.

NOTE 2: The Loop on Error option has one characteristic that could be confusing. If for example, the option is enabled and an Error occurs, the Error message will be displayed as usual, and the test will be repeated. But, the Error message is only displayed for about a second, so if the test starts Passing, the Diagnostic may appear to hang since no messages are being displayed and the Test Step number is remaining constant. The Diagnostic is not hung up, it is in fact repeating the same Test Step without Error. Pressing the CONTROL key, or disabling the Loop on Error Parameter will allow the Diagnostic execution to proceed.

Display Error Messages

This parameter controls whether or not the Error messages are displayed when Errors occur.

Normally when an Error occurs, and this option is set to YES, a message describing the Error is displayed for about a second, then the message is cleared. For most testing situations this is the desired response.

If a test is running that is rather lengthy, such as a RAM addressing test, and there are many Errors, the screen will display many Error messages. Each time a message is displayed the Diagnostic is paused, and this actually increases the Total Test Time. If the Display Error Messages is set to NO, this will decrease the Total Test Time.

If the unit is to be run unattended (i.e. it is not necessary to view every Error message and the maximum number of test cycles desired), this parameter should be set to NO. The total number of Errors can be displayed at a later time by pressing the DATA key.

NOTE: When the Display Error Messages is set to NO, the Diagnostic module that is currently executing still calls the Error tabulation routine, so every Error is counted and tabulated.

Number of Times to Repeat Test(s)

This parameter controls the number of times a test is performed. The default is 1. This means when the test or tests are started by pressing the NEXT key, testing is executed one time and the Diagnostic will pause.

If several test repeats or continuous testing is desired, any number from 1 to 65,535 can be selected. Enter this parameter by positioning the cursor, pressing the NEXT key, entering a number with 1 to 5 digits, and again pressing the NEXT key. (If 5 digits are entered, the terminating NEXT key need not be pressed.)

For example if the count desired is 158, press NEXT, 1, 5, 8, NEXT.
If a number larger than 65,535 is entered, the program will request you to re-enter the number.

NOTE: If the repeat count is more than one, DIAG will cycle through all Subtests of all Active boards and then repeat the cycle until the repeat count has been reached.

At any time during this execution, the DATA key may be pressed to view the Pass/Error history then the PREVIOUS key will resume execution. The EDIT key may also be pressed to change any of the parameters. The PREVIOUS key will then resume execution.

Test Drive A, Test Drive B

This parameter refers to the Floppy Disk Drive tests for Disk Drives A and B. If a Drive is selected, a Disk Write/Read test will be performed on that Drive, and a "scratch" Disk must be used since all data on that Disk will be destroyed.

The default selections are Drive A = NO, Drive B = YES. The Diagnostic Disk is residing in Disk Drive A, and a "scratch" Disk should be residing in Disk Drive B. With the default selections, no operator actions are required. Drive B is tested, and Drive A is not tested.

If both Disk Drives are to be tested, the parameter options must be changed to Drive A = YES, and Drive B = YES. Each time DIAG is ready to test Disk Drive A, the Diagnostic Disk must be removed, and a "scratch" Disk placed in the Drive. When the test is complete, the sratch Disk will have to be removed from Drive A, and the Diagnostic Disk re-inserted.

This procedure requires actions to be performed by the operator, and the RUN OPERATOR ACTIONS parameter must be enabled. This will be explained later.

NOTE: A "scratch" Disk is defined as a new or fairly new Floppy Diskette, that has been "formatted" using the K205 Disk Operating System Format command. The Write Protect slot must not be covered. The Disk used should not contain any important data or programs, since the process of Formatting and the Disk Drive testing destroys all data on the Diskette.

Test Side 0, Test Side 1

This parameter also refers to the Floppy Disk Drives testing. Each Disk Drive has two sides, Side 0 and Side 1. Normally parameters 7 and 8 will be YES, and both sides will be tested during the Floppy Disk testing.

If for example, Disk Drive B is having Errors on Side 1, and no Errors on Side 0, setting the TEST SIDE 0 option to NO will allow for more frequent testing of Side 1 of the Disk Drive, and give more Pass/Fail information at a quicker rate.

Run Operator Action Tests

Some of the tests in the Diagnostic modules require the operator to perform certain actions. One example is the testing of Disk Drive A requires the operator to remove the Diagnostic Disk and insert a "scratch" Disk, allow the test to run, then re-insert the Diagnostic Disk.

Other actions might be the installation of RS-232 wrap-back connectors, the testing of the Keys on the K205 Keyboard, GPIB Testing, etc.

If a unit is to run the Diagnostics unattended, this parameter should be set to NO, and the specific tests that require operator actions will not be performed.

PASS/ERROR TABLUATION (DATA KEY)

At anytime during the Diagnostic Execution the number of Passes and Errors can be displayed by pressing the DATA key. Pressing the PREVIOUS key will return to the previous Menu or executions. A list of the boards in the system will be displayed, as well as the total number of Errors as follows:

Number of Errors Cycle Through All Tests	
Keybd/Display	0
Data Board A	0
Data Board B	0
Data Board C	0
Control Board	0
Clock Board	0
Threshold Board	0
Storage Controller Board	0

There are two fields that are highlighted by the cursor, they are "Errors" and "Cycle Through All Tests". If the cursor is over Errors, pressing the NEXT key will change the display to the number of Passes, (changing Errors to Passes). Pressing the NEXT key again will change back to the Error display.

This Errors/Passes display shows the total accumulative Errors and Passes for each board in the K205 System. If a board is not in the system, or it was forced Inactive, the Pass and Error count will be 0 for that board. Otherwise, the number of times DIAG tested the board will be displayed for the Passes, and the total number, (if any), of Errors will be displayed.

If the down arrow key is entered this will move the cursor into the "Cycle Through All Tests" field, and pressing the NEXT key will display the total Errors/Passes for each Subtest of the Keyboard/Display Board. Pressing the NEXT key will then display the total Errors/Passes for each Subtest of Data Board A.

Consecutively pressing of the NEXT key will display the Data Board B, Data Board C, Control Board, Clock Board, Threshold Board, Storage Controller Board, and then finally back to the Board Level Error/Pass Display.

If for example, you wish to view information about Data Board A, do the following steps:

1. Press the DATA key to display the Board list and total Error count.
2. Press the NEXT key to display the Board list and total Pass count.
3. Press the down arrow key and press the NEXT key twice to display the Data Board A Subtest Pass count.

4. Press the up arrow key and then the NEXT key to display the Data Board A Subtest Error count.

5. Press the PREVIOUS key to return to the previous Menu.

DIAGNOSTIC RE-INITIALIZATION AND DIAGNOSTIC EXIT TO SYSTEM

General

When the Diagnostic Modules are executed, the Pass/Fail information is accumulated ; pressing the DATA key will display this information.

If a "fresh" start of the Diagnostic is desired, with the Pass/Error information set to 0, this can be achieved by entering the Main Menu by pressing the PREVIOUS key, and then pressing the PREVIOUS key again. This will set up the default Parameters, and set all Pass/Error information to 0.

NOTE: Be careful using the PREVIOUS key while in Main Menu, as it would be easy to re-initialize the Diagnostic by accident, and lose all the Pass/Error information that was accumulated.

Exiting the Diagnostic

When the K205 Logic Analyzer is powered on, it goes through its power on Diagnostics and comes up in the Default Menu. While in this menu, if you press the "F2" key, the power on diagnostics are repeated.

While the K205 Diagnostic Operating System is under Execution, it is possible to exit back to the Default Menu of the Logic Analyzer. This is done by pressing the "F2" key three consecutive times. This will cause any Diagnostic execution to be aborted, and the K205 will go through the power on diagnostics and come up in the Default Menu.

Pressing the "F2" key three consecutive times has the same effect as powering off the K205, and then powering it back on, without the need to remove the Floppy Diskettes.

NOTE: The "F2" key must be pressed three consecutive times to avoid an accidental exit from the Diagnostic Operating System. Any other keys pressed between the three "F2" keys voids out the exit.

SUMMARY OF K205 DIAGNOSTIC OPERATING SYSTEM KEYS

The K205 Diagnostic will recognize the following keys:

Key	Menu or Execution	Function
NEXT	Main Menu	Execute Diagnostic.
	Subtest Menu	Execute Diagnostic.
	HALTED ON ERROR	Resume Diagnostic execution.
	Parameter Menu	Change selected option.
	Pass/Error Display	Change Error display to Pass display, Cycle through Subtest lists.
PREVIOUS	Main Menu	Re-initialize Diagnostic.
	Subtest Menu	Return to Main Menu.
	Parameter Menu	Return to previous Menu or execution.
	Pass/Error Display	Return to previous Menu or execution.
EDIT	Any Menu or execution	Display the Parameter options.
DATA	Any Menu or execution	Display the Pass/Error information.
STOP	Any execution	Abort current test.
	HALTED ON ERROR	Abort current test.
FIELD (arrows)	Main Menu	Activate/Inactivate a Board, or Select a Board for testing.
	Subtest Menu	Select a Single Test or all Tests.
	Parameter Menu	Select a parameter.
	Pass/Error Display	Change fields for Errors/Passes, or cycle through all Subtest lists.
CONTROL	Looping on Error	Skip out of current Subtest and proceed to the next Subtest.
F2	Any Menu or execution	Three consecutive key-strokes causes an EXIT from the Diagnostics and cold starts the K205 Logic Analyzer.

K205 KEYBOARD/DISPLAY BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes subtests that are executed on the K205 keyboard/ display board, how error reporting is done, and the concept behind each subtest program.

There are eight subtests written for the keyboard/ display board. Each of the subtests are described individually on the pages which follow. Loop on error, error count, and pass count update are incorporated into each subtest. Details for selecting the various test options and parameters for controlling the diagnostic monitor are described in the Introduction for Chapter 5.

All Error Messages are preceded by a "*" while Information Messages use the ">" prefix.

Early exit of each subtest is accomplished by pressing the "STOP" key.

ASSUMPTIONS

This series of tests assumes that the following boards are installed and are operational:

1. MPU
2. Threshold/GPIB/RS-232
3. Clock
4. Control

SUBTEST CATEGORIES

1. Keyboard Test
2. Interrupt Controller (8259) Test
3. Clock/Calendar (5832) Test
4. Video RAM Data Test
5. Video RAM Address Test
6. 6116 RAM Data Test
7. 6116 RAM Address Test
8. Beeper Exercise

ERROR COUNT CATEGORIES

1. Subtest 1 Error Count
2. Subtest 2 Error Count
3. Subtest 3 Error Count
4. Subtest 4 Error Count
5. Subtest 5 Error Count
6. Subtest 6 Error Count
7. Subtest 7 Error Count
8. Subtest 8 Error Count

TITLE: KEYBOARD TEST

TARGET LOGIC: 8E, 14E, 13E, 10E and keyboard interface matrix

PURPOSE: The keyboard logic is functionally tested by pressing a specified key on the front panel, reading the corresponding I/O port from buffer (10E), and then verifying the key data to the expected data.

TEST DESCRIPTION: There are 48 keys on the front panel; the corresponding I/O Port, 1xh are arranged as follows:

a. x=0 if key is located at column 1 in the front panel
b. x=2 if key is located at column 2 in the front panel
c. x=4 if key is located at column 3 in the front panel
d. x=6 if key is located at column 4 in the front panel
e. x=8 if key is located at column 5 in the front panel
f. x=a if key is located at column 6 in the front panel
h. x=c if key is located at column 7 in the front panel
i. x=e if key is located at column 8 in the front panel.

There are 6 key data read from the buffer (10e),they are arranged as follows:

a. the key data read=feh if the key is located at row 1 in the front panel
b. the key data read=fdh if the key is located at row 2 in the front panel
c. the key data read=fbh if the key is located at row 3 in the front panel
d. the key data read=f7h if the key is located at row 4 in the front panel
e. the key data read=efh if the key is located at row 5 in the front panel
f. the key data read=dfh if the key is located at row 6 in the front panel

The following information message is displayed before each key is tested:

>Press key labeled: ????????????

Where ????????????? could be 1 character, for example, "0" through "9", "a" through "f", or up to 13 characters, for example, "TRACE CONTROL" in the domain of 48 defined keys.

TEST STEP INFORMATION:

Test Step	Key Tested
1	NEXT
2	PREVIOUS
3	FORMAT
4	CLOCKS
5	TRACE CONTROL
6	ARM MODE
7	UP ARROW
8	LEFT ARROW
9	MEM A
10	DATA
11	TIMING

Test Step	Key Tested (cont'd)
12	GRAPH
13	RIGHT ARROW
14	DOWN ARROW
15	MEM B
16	A->B
17	SEARCH
18	COMPARE
19	CONTROL
20	REF
21	C
22	8
23	4
24	0
25	SHIFT
26	HELP
27	D
28	9
29	5
30	1
31	I/O
32	"X"
33	E
34	A
35	6
36	2
37	EDIT
38	INS
39	F
40	B
41	7
42	3
43	ARM
44	STOP
45	F1
46	F2
47	F3
48	F4

ERROR MESSAGE:

If a key data error occurs, the following message is displayed:

```
*Test FAILED--Test Step    ss
 Keyboard Error
 Expected Keycode   = eeh
 Keycode Found      = ddh
 Key Data Code Read = "?????????????"
```

where ss should be 1 through 48
ee should be 1 through 48
dd should be be 1 through 48

TITLE: INTERRUPT CONTROLLER TEST

PURPOSE: The interrupt logic is functionally tested by selecting each interrupt on the 8259 controller and causing each interrupt to occur. As each interrupt is generated, the 8259 receives the interrupt then outputs a vector for the 8086 processor. At these vectors are routines which set diagnostic flags. These flags are examined to determine if the interrupt actually took place. The source of the interrupts are then turned off, and the flags are cleared. After a small amount of time the flags are re-examined to determine if the source of the interrupt has actually been disabled. If a flag is found to be set then an error message is displayed.

TARGET LOGIC: 4E, 2E, 8E, 10E, 9D, and 10D

TEST DESCRIPTION: The following table indicates the interrupt source and line for the diagnostic test step:

TEST STEP INFORMATION:

Test Step	Interrupt from	On Board	Interrupt Line
1	GPIB	Threshold	intr 1
2	RS-232	Threshold	intr 2
3	AUX	Threshold	intr 3
4	Total trace time clock (timer #0)	Clock	intr 4
5	(Simulated from software)		not currently assigned
6	Time of day	Display	intr 6
7	Disk	Storage Controller	intr 7

ERROR MESSAGE:

If an error occurs, the following messages are displayed:

*Test FAILED--Test Step z
Intr 0z Not Generated.

where z = 1 - 7

*Test FAILED--Test Step z
Unexpected Interrupt 0z Generated.

where z = 1 - 7

Keyboard/Display Diagnostic Subtest 3

TITLE: CLOCK/CALENDAR TEST

PURPOSE: This subtest verifies operation of the 5832 clock/calendar by saving the current time, then exercising the component by setting the time. The time is then read back and verified. If test is successful, it indicates the 5832 is operating properly.

The time is set so the next second time interval causes a rollover. An example of a rollover is if the minutes counter was set to 59. When minutes are advanced then the minutes counter becomes zero and the hours count is incremented by one. This rollover process continues until the years counter rolls over to 00 (from 99).

TARGET LOGIC: 2D, 2E, 3D, 4D, 5D and 7D

TEST DESCRIPTION: Operations are exercised on the clock calendar components according to the following table:

TEST STEP INFORMATION:

Test Step	Operation
1	Read current time, save for last step
2	Set clock to: Jan. 1, 1900 @00:00:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1900 @00:01:00
3	Set clock to: Jan. 1, 1900 @00:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1900 @01:00:00
4	Set clock to: Jan. 1, 1900 @23:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 2, 1900 @00:00:00

Test Step	Operation (cont'd)
5	Set clock to: Jan. 31, 1900 @23:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Feb. 1, 1900 @00:00:00
6	Set clock to: Dec. 31, 1900 @23:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1901 @00:00:00
7	Set clock to: Dec. 31, 1999 @23:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1900 @00:00:00

NOTE: Exiting this test via the STOP key restores the time saved in step 1. If power is removed during steps 2 - 7, the time is lost.

ERROR MESSAGE:

If the time read does not match the time expected, the following error message is displayed:

```
*Test FAILED--Test Step          x
Clock/Calendar Error
          year month  day hour  minute  second
Expected: aaa  bbb    ccc ddd   eee     fff
    Read: ggg  hhh    iii jjj   kkk     lll
```

where aaa, ggg = 000 - 999
bbb, hhh = 001 - 012
ccc, iii = 001 - 031
ddd, jjj = 000 - 023
eee, kkk = 000 - 059
fff, lll = 000 - 059

Keyboard/Display Diagnostic Subtest 4

TITLE: VIDEO RAM DATA TEST

PURPOSE: This subtest verifies that the Keyboard/Display Board does not prevent normal operation of the MPU RAM dedicated to video display.

TARGET LOGIC: 7A, 7B, 7C, 8A, 8B, 8C, 9A, 9B, 9C, 10A and 10B dedicated RAM on MPU Board used for video

TEST DESCRIPTION: Although the RAM under test is on the MPU Board, the Display Board uses this memory to create an image sent to the screen. Various data patterns are written to the MPU memory and read back. The data written is compared to the data read and if a miscompare is detected an error message is displayed. This continues until all the data patterns listed below have been tried.

TEST STEP INFORMATION:

Test Step	Value Written
1	00H
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

NOTE: This memory physically starts at location 0100h

ERROR MESSAGE:

If an error occurs during this subtest the following message is displayed:

```
* Test FAILED--Test step   xx
RAM Data Error
Value Written = aaH
Value Read    = bbH
Address Count = ccccH
```

where aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 3FFF

Keyboard/Display Diagnostic Subtest 5

TITLE: VIDEO RAM ADDRESS TEST

PURPOSE: This subtest verifies that the Keyboard/Display Board does not prevent normal operation of the MPU RAM dedicated to video display.

TARGET LOGIC: 7A, 7B, 7C, 8A, 8B, 8C, 9A, 9B, 9C, 10A and 10B
RAM located on MPU Board used for video,

TEST DESCRIPTION: All of the RAM in this test is preset to zero then the indicated address is written with the value 0aah. All of the RAM is then read to verify that the indicated address is the only data element that was set to 0aah.

TEST STEP INFORMATION:

Test Step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H

NOTE: This memory physically starts at location 0100h

ERROR MESSAGE:

If an error occurs during this subtest, the following message is displayed:

```
* Test FAILED--Test Step     xx
RAM Data Error
Value Written = aah
Value Read    = bbh
Address Count = ccccch
```

where aa = 00 - ff
bb = 00 - ff
cccc = 0000 - 3fff

TITLE: 6116 RAM DATA TEST

PURPOSE: This subtest verifies operation and integrity of the 6116 RAMs on the keyboard/display board by writing to the memory several different data patterns. This memory is then read back and compared to the value written. If a miscompare occurs then an error message is displayed. This process is repeated for all of the 6116 memory until all the patterns listed below have been tried.

TARGET LOGIC: 1B, 3B, 3C, 4C, 5B, 6B, 5E, 6E, 5C and 6D

TEST DESCRIPTION: The following is a summary of the data written to the RAM during each test step:

TEST STEP INFORMATION:

Test Step	Value Written
1	00H
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

NOTE: This memory physically starts at location 040000h

ERROR MESSAGE:

If an error occurs during this subtest, the following message is displayed:

```
* Test FAILED--Test Step   xx
RAM Data Error
Value Written = aaH
Value Read    = bbH
Address Count = ccccH
```

where aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 3FFF

TITLE: 6116 RAM ADDRESS TEST

PURPOSE: This subtest verfies the operation and integrity of the 6116 RAMs on the keyboard/display board. All of the RAM in this test is preset to zero then the indicated address is written with the value 0aah. All of RAM is then read to verify that the indicated address is the only data element that was set to 0aah.

TARGET LOGIC: 1B, 3B, 3C, 4C, 5B, 6B, 5E, 6E, 5C and 6D

TEST DESCRIPTION: All RAM is preset to zero, then the indicated address is written with the value 0aah. All of RAM is then read to verify the written data.

TEST STEP INFORMATION:

Test Step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H

NOTE: This memory physically starts at location 040000h

ERROR MESSAGE:

If an error occurs during this subtest, the following message is displayed:

```
* Test FAILED--Test step    xx
RAM Data Error
Value Written = aaH
Value Read    = bbH
Address Count = ccccH
```

where aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 3FFF

Keyboard/Display Diagnostic Subtest 8

TITLE: BEEPER EXERCISE TEST

PURPOSE: This subtest exercises the beeper circuitry. there are no error messages generated by this routine as there is no way to verfy operation except via audio monitoring.

TARGET LOGIC: 15E, 16E, 17E and 18E

TEST DESCRIPTION: The beeper is activated by loading p0-p3 on IC with the duration value, then the line labeled cp is pulsed. The beeper is set to various durations as given in the following table:

TEST STEP INFORMATION:

Test Step	Duration
1	.1 sec
25	1.5 sec

ERROR MESSAGE:

There are no error messages for this subtest. Also note that since no errors are possible, "loop on error" and "halt on error" do not function.

K205 DATA BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes subtests that are performed by the K205 Data Board Diagnostic. The target hardware is presented, as well as a general description of each subtest, a list of information for each test step, and a description of Error Messages that may be printed for the subtest results.

The K205 Data Board Diagnostic is a board level test of the board operations that run under the K205 Diagnostic Operating System. The diagnostic can test from 1 to 3 Data Boards in the system. These correspond to Data Boards A, B and C. In order for the Diagnostic to run properly, the board under test must be installed on the Mother Board, (not on an extender card). The internal probe input cables must be connected to J1 and J2, and the external probes installed. All of the channels of all probes must be free from connection to anything (i.e. they must be allowed to float). Also, all of the other boards must be installed in the K205 system.

NOTE: The internal probe input cables are too short for the board to be installed on an extender card. If extension cables are used, then an extender card may be used.

Several of the subtests use a sequence of 24 Data patterns to write, read and verify an I/O port or Memory Address. These Data patterns verify that all 16 Data Bits are functional and completely independent of each other. These 24 Data patterns are as follows:

0000H, 5555H, AAAAH, CCCCH, 3333H, 6666H, 9999H, FFFFH,
0001H, 0002H, 0004H, 0008H, 0010H, 0020H, 0040H, 0080H,
0100H, 0200H, 0400H, 0800H, 1000H, 2000H, 4000H, 8000H.

When writing these Data patterns to an I/O port such as the Sample Register or the Pipeline Registers, the Data value can be randomly accessed. The ECL RAM Memory on the other hand is essentially a 512 byte FIFO. All 512 locations are accessed at the same I/O address, (i.e. 0C6H for writes, and 0C0H for reads). The RAM's addressing is accomplished by sequential reads from, or writes to the RAM. Address counters on the board are incremented each time a RAM access (i.e. a Sample Clock) occurs.

The RAM actually requires 515 Sample clocks to get 512 words of data to the RAM. The three extra clocks are required to get the Data through the pipeline. After the 512th clock, the 512th Data value resides in the Sample Register. One more clock shifts it to the New Pipe Register. An additional clock shifts it to the Old Pipe Register, and the last clock writes it to RAM.

NOTE: When an I/O address is specified for explanation, the addresses for Data Board A are used. These addresses would only apply if Data Board A was being tested. Data Board B addresses are 0DxH, and Data Board C are 0ExH.

SUBTEST CATAGORIES

There are thirteen Subtests that are performed by the Data Board Diagnostic. These are categorized as follows:

1. Force Conditions Test
2. Data Path Test
3. Clocking Disable Test
4. Latch Bits 0-7 Test
5. Latch Bits 8-F Test
6. Glitch Bits 0-7 Test
7. Glitch Bits 8-F Test
8. Multiplex Select Test
9. Pipeline Shift Test
10. RAM Data Integrity
11. RAM Addr Integrity
12. Trace Conditions Test
13. Recirculate RAM Test

ERROR COUNT CATEGORIES

The Error Count Display information is a one for one match with the Subtest list above. The K205 Diagnostic Operating System will display the "Subtest n" instead of the actual test name.

Subtest 1	(Force Conditions Test)
Subtest 2	(Data Path Test)
Subtest 3	(Clocking Disable Test)
Subtest 4	(Latch Bits 0-7 Test)
Subtest 5	(Latch Bits 8-F Test)
Subtest 6	(Glitch Bits 0-7 Test)
Subtest 7	(Glitch Bits 8-F Test)
Subtest 8	(Multiplex Select Test)
Subtest 9	(Pipeline Shift Test)
Subtest 10	(RAM Data Integrity)
Subtest 11	(RAM Addr Integrity)
Subtest 12	(Trace Conditions Test)
Subtest 13	(Recirculate RAM Test)

TITLE: FORCE CONDITIONS TEST

TARGET LOGIC:

6H
6M 7L 10L 9K 7F 5F 8F 9H 6L
8K 7K 9M 8L 12M 13M
1M 2M 3M 11M 8K
7K 9M 8L 8M 10M

TEST DESCRIPTION: This subtest writes various commands to the Data Board and expects certain status values to exist. The commands are written to ports 0C2H and 0C4H. The status is read back from port 0C8H.

This test does not require any boards other than the MPU to be installed in the system. Specifically, it requires no clocking from the Clock Board.

TEST STEP INFORMATION:

Step	Status Expected
1	45H
2	65H
3	75H
4	F5H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 4.

hmsg is the Error heading message:

Not Halt, Mem full, ExpWrIow 02 Error
Multiphase Mode Clear Error
Async Mode Clear Error
Freeze Memory Clear Error

aaaa is the I/O address of the Data Board:

0C8H for Data Board A Status Register,
0D8H for Data Board B Status Register,
0E8H for Data Board C Status Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 2

TITLE: DATA PATH TEST

TARGET LOGIC:

6M 7L 10L 9K 6F 5H 9F
2D 1D 2C 1C 4D 3C 4C 3D
11D 10D 11C 10C 13D 12C 13C 12D
2H 1H 4H 3H 11H 10H 13H 12H
2J 1J 4J 3J 11J 10J 13J 12J
8K 7K 9M 8L 5K 6J
10K 11L 12L 13L
13M 12M 1M 2M 3M 11M 8M 10M

TEST DESCRIPTION: This subtest checks the Data Bus path of the Data Board for functionality and Data Bit uniqueness. Data is transferred by sending output to the Diagnostic Latch at I/O address 0C6H, issuing a Sample Clock, receiving input from the Sample Register at I/O address 0C6H, and comparing Data. Since the Glitch Mode and Latch Mode are both disabled, the Data will slip through to the Sample Registers without the need for a Latch Clock.

The Clock Board is required to run this test. The "Sample Clock", P1-42 is used to clock the data to the Sample Register. This is achieved by doing a "KICK$CLOCK", which writes a "1" to Data bit D0 of Write Register 8, (0B8H), of the Clock Board.

The majority of the subsequent subtests use this Data Path to exercise various features and functions of the Data Board. So if there are any errors in this test, there are bound to be many failures that follow.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	0C6H, Diagnostic Latch	0C6H, Sample Register
2	5555H	0C6H, Diagnostic Latch	0C6H, Sample Register
3	AAAAH	0C6H, Diagnostic Latch	0C6H, Sample Register
4	CCCCH	0C6H, Diagnostic Latch	0C6H, Sample Register
5	3333H	0C6H, Diagnostic Latch	0C6H, Sample Register
6	6666H	0C6H, Diagnostic Latch	0C6H, Sample Register
7	9999H	0C6H, Diagnostic Latch	0C6H, Sample Register
8	FFFFH	0C6H, Diagnostic Latch	0C6H, Sample Register
9	0001H	0C6H, Diagnostic Latch	0C6H, Sample Register
10	0002H	0C6H, Diagnostic Latch	0C6H, Sample Register
11	0004H	0C6H, Diagnostic Latch	0C6H, Sample Register
12	0008H	0C6H, Diagnostic Latch	0C6H, Sample Register
13	0010H	0C6H, Diagnostic Latch	0C6H, Sample Register
14	0020H	0C6H, Diagnostic Latch	0C6H, Sample Register
15	0040H	0C6H, Diagnostic Latch	0C6H, Sample Register
16	0080H	0C6H, Diagnostic Latch	0C6H, Sample Register
17	0100H	0C6H, Diagnostic Latch	0C6H, Sample Register
18	0200H	0C6H, Diagnostic Latch	0C6H, Sample Register
19	0400H	0C6H, Diagnostic Latch	0C6H, Sample Register
20	0800H	0C6H, Diagnostic Latch	0C6H, Sample Register
21	1000H	0C6H, Diagnostic Latch	0C6H, Sample Register
22	2000H	0C6H, Diagnostic Latch	0C6H, Sample Register
23	4000H	0C6H, Diagnostic Latch	0C6H, Sample Register
24	8000H	0C6H, Diagnostic Latch	0C6H, Sample Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Data Path Diag to Sample Reg Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:
0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

TITLE: CLOCK DISABLE TEST

TARGET LOGIC: 5K 8J 6J 5L
6H 5A 6A 8A 9A
All Logic listed in Subtest 2

TEST DESCRIPTION:

This subtest checks the different ways of clocking the Data Board, and the different ways of disabling the clocking.

In Single Phase Mode the Sample Clock, P1-42 is used for all clocking on the Data Board. If the Multiphase Mode is selected, the Sample Clock, P1-42 is used for the Sample Register, and the Control Clock, P1-46 is used for the RAM, Pipelines and Address Counters.

A Condition called "Force Clocks" will cause all Sample Clocks and all Control Clocks to be ignored. Also a condition called "Halted" will disable these clocks.

This test also checks the Address Reset--Memory Full function. The address counters are reset by toggling W4B12. The Memory is "filled" by clocking the address counters 512 times.

TEST STEP INFORMATION:

Step	Mode of Phase	Force Clocks	Data Expected
1	Single Phase	inactive	5555H
2	Multi Phase	inactive	AAAAH
3	Single Phase	active	0000H
4	Multi Phase	active	0000H

Step	"HALTED/"	MEMORYFULL	Status
5	high	low	0001H
6	low	high	0004H

Step	Mode of Phase	Force Clocks	Halt When Full	Data Expected
7	Single Phase	inactive	active	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 7.

hmsg is the Error heading message:

- Force Clocks Enable Data move Error,
- Force Clocks Disable Data move Error,
- 155 En2 Memory Not Full Status Error,
- 155 En2 Mem-Full/Halt Status Error,
- Halt Freeze Sample Register Error.

aaaa is the I/O address of the Data Board:

- 0C6H for Data Board A Sample Register,
- 0C8H for Data Board A Status Register,
- 0D6H for Data Board B Sample Register,
- 0D8H for Data Board B Status Register,
- 0E6H for Data Board C Sample Register,
- 0E8H for Data Board C Status Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 4

TITLE: LATCH DATA BITS 0-7 TEST

TARGET LOGIC: 5F
5L
2H 1H 4H 3H 11H 10H 13H 12H

Diagnostic Latch Clock P1-44 (From Clock Board)

All hardware used in Data Path Test.

TEST DESCRIPTION:

This tests the latch mode of 10130 latches of the lower 8 bits, with the upper eight bits in transparent mode. The Latch Clock 0-7 feeds the common Enable input to the 10130's. This input is held high, and pulsed low to latch the current data from the "D" to the "Q". The Glitch is disabled so the other Enable input is held low. The upper bits 8-F are not latched, the Data slips through the "D" to the "Q".

If there are any errors in this test, but the Data Path Test passed, the failure is probably in the Latch Clock or the 10130's.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	0C6H, Diagnostic Latch	0C6H, Sample Register
2	5555H	0C6H, Diagnostic Latch	0C6H, Sample Register
3	AAAAH	0C6H, Diagnostic Latch	0C6H, Sample Register
4	CCCCH	0C6H, Diagnostic Latch	0C6H, Sample Register
5	3333H	0C6H, Diagnostic Latch	0C6H, Sample Register
6	6666H	0C6H, Diagnostic Latch	0C6H, Sample Register
7	9999H	0C6H, Diagnostic Latch	0C6H, Sample Register
8	FFFFH	0C6H, Diagnostic Latch	0C6H, Sample Register
9	0001H	0C6H, Diagnostic Latch	0C6H, Sample Register
10	0002H	0C6H, Diagnostic Latch	0C6H, Sample Register
11	0004H	0C6H, Diagnostic Latch	0C6H, Sample Register
12	0008H	0C6H, Diagnostic Latch	0C6H, Sample Register
13	0010H	0C6H, Diagnostic Latch	0C6H, Sample Register
14	0020H	0C6H, Diagnostic Latch	0C6H, Sample Register
15	0040H	0C6H, Diagnostic Latch	0C6H, Sample Register
16	0080H	0C6H, Diagnostic Latch	0C6H, Sample Register
17	0100H	0C6H, Diagnostic Latch	0C6H, Sample Register
18	0200H	0C6H, Diagnostic Latch	0C6H, Sample Register
19	0400H	0C6H, Diagnostic Latch	0C6H, Sample Register
20	0800H	0C6H, Diagnostic Latch	0C6H, Sample Register
21	1000H	0C6H, Diagnostic Latch	0C6H, Sample Register
22	2000H	0C6H, Diagnostic Latch	0C6H, Sample Register
23	4000H	0C6H, Diagnostic Latch	0C6H, Sample Register
24	8000H	0C6H, Diagnostic Latch	0C6H, Sample Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Latch Data bits 0-7 Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:
0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 5

TITLE: LATCH DATA BITS 8-F TEST

TARGET LOGIC:

5F
5L
2H 1H 4H 3H 11H 10H 13H 12H

Diagnostic Latch Clock P1-44 (From Clock Board)

All hardware used in Data Path Test.

TEST DESCRIPTION:

This subtest is identical to the previous test except that the upper Data bits 8-F are tested instead of the lower bits 0-7.

The test verifies the latch mode of 10130 latches the upper 8 bits, with the lower eight bits in transparent mode. The Latch Clock 8-F feeds the common Enable input to the 10130's. This input is held high, and pulsed low to latch the current data from the "D" to the "Q". The Glitch is disabled so the other Enable input is held low. The lower bits 0-7 are not latched, the Data slips through the "D" to the "Q".

If there are any errors in this test, but the Data Path Test passed, the failure is probably in the Latch Clock or the 10130's.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	0C6H, Diagnostic Latch	0C6H, Sample Register
2	5555H	0C6H, Diagnostic Latch	0C6H, Sample Register
3	AAAAH	0C6H, Diagnostic Latch	0C6H, Sample Register
4	CCCCH	0C6H, Diagnostic Latch	0C6H, Sample Register
5	3333H	0C6H, Diagnostic Latch	0C6H, Sample Register
6	6666H	0C6H, Diagnostic Latch	0C6H, Sample Register
7	9999H	0C6H, Diagnostic Latch	0C6H, Sample Register
8	FFFFH	0C6H, Diagnostic Latch	0C6H, Sample Register
9	0001H	0C6H, Diagnostic Latch	0C6H, Sample Register
10	0002H	0C6H, Diagnostic Latch	0C6H, Sample Register
11	0004H	0C6H, Diagnostic Latch	0C6H, Sample Register
12	0008H	0C6H, Diagnostic Latch	0C6H, Sample Register
13	0010H	0C6H, Diagnostic Latch	0C6H, Sample Register
14	0020H	0C6H, Diagnostic Latch	0C6H, Sample Register
15	0040H	0C6H, Diagnostic Latch	0C6H, Sample Register
16	0080H	0C6H, Diagnostic Latch	0C6H, Sample Register
17	0100H	0C6H, Diagnostic Latch	0C6H, Sample Register
18	0200H	0C6H, Diagnostic Latch	0C6H, Sample Register
19	0400H	0C6H, Diagnostic Latch	0C6H, Sample Register
20	0800H	0C6H, Diagnostic Latch	0C6H, Sample Register
21	1000H	0C6H, Diagnostic Latch	0C6H, Sample Register
22	2000H	0C6H, Diagnostic Latch	0C6H, Sample Register
23	4000H	0C6H, Diagnostic Latch	0C6H, Sample Register
24	8000H	0C6H, Diagnostic Latch	0C6H, Sample Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Latch Data bits 8-F Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:
0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

TITLE: GLITCH DATA BITS 0-7 TEST

TARGET LOGIC:

2E 1E 2F 1F
4E 3F 4F 3E
11E 10E 11F 10F
13E 12F 13F 12E
2H 1H 4H 3H
11H 10H 13H 12H

All hardware in the Data Path Test.

TEST DESCRIPTION:

This subtest tests the Glitch capture feature of the Data boards by enabling the Glitch circuitry which uses the "Set" and "Reset" pins on the 10130's, instead of the "D" inputs to send the Data from the 10121 Multiplexers to the "Q" output. The individual Enable pins on the 10130's are held high so that any "clocking" from the Diagnostic Latch Clock is disabled. (No effect).

Each output instruction to the Diagnostic bits port 0C6H, latches the Data in the Glitch latches. A Sample Clock is required to send the Data through to the Sample Register. A maximum cf two Data values may be output to the Diagnostic bits port before data overrun occurs.

The way that this circuitry is tested, is two consecutive Output instructions are performed with different Data. The first Data is checked at the Sample register after issuing a single Sample Clock. Another Sample Clock will present the Second Data to the Sample Register.

In this test, only Data bits 0-7 are in the Glitch Mode. The upper bits 8-F slip through the 10130's because both of the enable pins are low, so "Q" follows "D".

TEST STEP INFORMATION:

Step	1st Data	2nd Data
1	0000H	------
2	0000H	0000H
3	0055H	0000H
4	00AAH	0000H
5	00CCH	0000H
6	0033H	0000H
7	0066H	0000H
8	0099H	0000H
9	00FFH	0000H
10	0001H	0000H
11	0002H	0000H

Step	1st Data	2nd Data (cont'd)
12	0004H	0000H
13	0008H	0000H
14	0010H	0000H
15	0020H	0000H
16	0040H	0000H
17	0080H	0000H
18	0000H	0000H
19	0000H	0000H
20	0000H	0000H
21	0000H	0000H
22	0000H	0000H
23	0000H	0000H
24	0000H	0000H
25	0000H	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Glitch Data Bits 0-7 Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 25.

aaaa is the I/O address of the Data Board:
0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 7

TITLE: GLITCH DATA BITS 8-F TEST

TARGET LOGIC:

2E 1E 2F 1F
4E 3F 4F 3E
11E 10E 11F 10F
13E 12F 13F 12E
2H 1H 4H 3H
11H 10H 13H 12H

All hardware in the Data Path Test.

TEST DESCRIPTION:

This subtest is similar to the Glitch Data Bits 0-7 except the upper bits are being tested.

This subtest checks the Glitch capture feature of the Data boards by enabling the Glitch circuitry which uses the "Set" and "Reset" pins on the 10130's, instead of the "D" inputs to send the Data from the 10121 Multiplexers to the "Q" output. The individual Enable pins on the 10130's are held high so that any "clocking" from the Diagnostic Latch Clock is disabled. (No effect).

Each output instruction to the Diagnostic bits port 0C6H, latches the Data in the Glitch latches. A Sample Clock is required to send the Data through to the Sample Register. A maximum of two Data values may be output to the Diagnostic bits port before data overrun occurs.

The way that this circuitry is tested, is two consecutive Output instructions are performed with different Data. The first Data is checked at the Sample register after issuing a single Sample Clock. Another Sample Clock presents the Second Data to the Sample Register.

In this test, only Data bits 8-F are in the Glitch Mode. The lower bits 0-7 slip through the 10130's because both of the enable pins are low, so "Q" follows "D".

TEST STEP INFORMATION:

Step	1st Data	2nd Data
1	0000H	------
2	0000H	0000H
3	5500H	0000H
4	AA00H	0000H
5	CC00H	0000H
6	3300H	0000H
7	6600H	0000H
8	9900H	0000H
9	FF00H	0000H

Step	1st Data	2nd Data (Cont'd)
10	0000H	0000H
11	0000H	0000H
12	0000H	0000H
13	0000H	0000H
14	0000H	0000H
15	0000H	0000H
16	0000H	0000H
17	0000H	0000H
18	0100H	0000H
19	0200H	0000H
20	0400H	0000H
21	0800H	0000H
22	1000H	0000H
23	2000H	0000H
24	4000H	0000H
25	8000H	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Glitch Data Bits 8-F Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 25.

aaaa is the I/O address of the Data Board:
0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

TITLE: PROBES/MULTIPLEX TEST

TARGET LOGIC:

8F
2B 1B 4B 3B 11B 10B 13B 12B
2D 1D 2C 1C 4D 3C 4C 3D
11D 10D 11C 10C 13D 12C 13C 12D

J1, J2, Internal Probe Cables, External Probe Cables

All of the hardware in the Data Path Test.

TEST DESCRIPTION:

This subtest checks the five Multiplexing Select Modes of the Data Board. The five modes are:

1. "NORMAL" mode. This samples the logic state at the inputs of J1 and J2. This logic state is set high or low by the external probes.

2. "DEMUX" mode. This is similar to the Normal Mode except the lower eight bits are mirrored into the upper eight bits.

3. "DIAGNOSTIC" select. This reads the Diagnostic bits Register.

4. "MEMORY" select. This reads the data that is currently residing in the ECL Memory, (Manual Recirculate).

5. NOTHING SELECTED. With all four select lines disabled, the Data lines should be pulled up to read OFFFFH.

This subtest requires the use of a known good Threshold Board and the installation of the external probes. The Normal Mode and the Demux Mode use the Threshold board to set different thresholds at the hybrid circuit in the probes.

TEST STEP INFORMATION:

Step	Data Expected	Multiplex	Lower Threshold	Upper Threshold
1	FFFFH	Normal	ECL	ECL
2	0000H	Normal	VARIABLE A	VARIABLE A
3	00FFH	Normal	ECL	VARIABLE A
4	FFFFH	Demux	ECL	ECL
5	0000H	Demux	VARIABLE A	VARIABLE A
6	FFFFH	Demux	ECL	VARIABLE A
7	F069H	Diagnostic	----------	----------
8	5AC3H	Memory	----------	----------
9	FFFFH	Floating	----------	----------

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 9.

hmsg is the Error heading message:

Normal ECL Threshold Mux Error,
Normal VARA F Threshold Mux Error,
Normal ECLVARA Threshold Mux Error,
Demux ECL Threshold Mux Error,
Demux VARA F Threshold Mux Error,
Demux ECLVARA Threshold Mux Error,
Diagnostic Select Mux Error,
Memory Select Mux Error,
Multiplexer Disable-Float Error.

aaaa is the I/O address of the Data Board:

0C6H for Data Board A Sample Register,
0D6H for Data Board B Sample Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

TITLE: PIPELINES SHIFT TEST

TARGET LOGIC: 2K 1K 3K 11K 12K 13K
2L 1L 3L 4L 10K 11L 12L 13L
5K

Sample Clock P1-42,

Control Clock P1-46, (from Clock Board).

All hardware in Data Path Test.

TEST DESCRIPTION:

This test checks the Data Board Pipeline. The Pipeline consists of a three step FILO, (first in last out), with "D" latches at each step that can be read. The steps are called the "Sample Register", the "New Pipe Register", and the "Old Pipe Register" respectively.

With each Pipeline Clock transition, the Old Pipeline Register Data is lost and receives its new data from the New Pipeline Register. The New Pipeline Register receives its new data from the Sample Register. The Sample Register receives its data from the 10130 Glitch Latches.

The Pipeline can receive it's clocking from either the Sample Clock if "Single Phase Mode" is selected, or from the Control Clock if "Multi Phase Mode" is selected. Test Steps 1 - 24 will use the Sample Clock, and Test Steps 25 - 48 will use the Control Clock.

TEST STEP INFORMATION:

Step	Sample Data	New Pipe Data	Old Pipe Data	Mode of Phase
1	0000H	0000H	0000H	Single Phase
2	5555H	0000H	0000H	Single Phase
3	AAAAH	5555H	0000H	Single Phase
4	CCCCH	AAAAH	5555H	Single Phase
5	3333H	CCCCH	AAAAH	Single Phase
6	6666H	3333H	CCCCH	Single Phase
7	9999H	6666H	3333H	Single Phase
8	FFFFH	9999H	6666H	Single Phase
9	0001H	FFFFH	9999H	Single Phase
10	0002H	0001H	FFFFH	Single Phase
11	0004H	0002H	0001H	Single Phase
12	0008H	0004H	0002H	Single Phase
13	0010H	0008H	0004H	Single Phase
14	0020H	0010H	0008H	Single Phase
15	0040H	0020H	0010H	Single Phase
16	0080H	0040H	0020H	Single Phase

Step	Sample Data	New Pipe Data	Old Pipe Data	Mode of Phase(Cont'd)
17	0100H	0080H	0040H	Single Phase
18	0200H	0100H	0080H	Single Phase
19	0400H	0200H	0100H	Single Phase
20	0800H	0400H	0200H	Single Phase
21	1000H	0800H	0400H	Single Phase
22	2000H	1000H	0800H	Single Phase
23	4000H	2000H	1000H	Single Phase
24	8000H	4000H	2000H	Single Phase
25	0000H	0000H	0000H	Multi Phase
26	5555H	0000H	0000H	Multi Phase
27	AAAAH	5555H	0000H	Multi Phase
28	CCCCH	AAAAH	5555H	Multi Phase
29	3333H	CCCCH	AAAAH	Multi Phase
30	6666H	3333H	CCCCH	Multi Phase
31	9999H	6666H	3333H	Multi Phase
32	FFFFH	9999H	6666H	Multi Phase
33	0001H	FFFFH	9999H	Multi Phase
34	0002H	0001H	FFFFH	Multi Phase
35	0004H	0002H	0001H	Multi Phase
36	0008H	0004H	0002H	Multi Phase
37	0010H	0008H	0004H	Multi Phase
38	0020H	0010H	0008H	Multi Phase
39	0040H	0020H	0010H	Multi Phase
40	0080H	0040H	0020H	Multi Phase
41	0100H	0080H	0040H	Multi Phase
42	0200H	0100H	0080H	Multi Phase
43	0400H	0200H	0100H	Multi Phase
44	0800H	0400H	0200H	Multi Phase
45	1000H	0800H	0400H	Multi Phase
46	2000H	1000H	0800H	Multi Phase
47	4000H	2000H	1000H	Multi Phase
48	8000H	4000H	2000H	Multi Phase

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address     = aaaaH
Data Read       = rrrrH
Data Expected   = eeeeH
Error Bit Map   = 0000000000000000B
Board Status X8 = iiiiH
```

Where:
ssss is the test step number in the range of 1 to 48.

hmsg is the Error heading message:
Sample Clock: Old Pipe Register Error
Sample Clock: New Pipe Register Error

ERROR MESSAGES: (Cont'd.)

Sample Clock: Sample Register Error
Control Clock: Old Pipe Register Error
Control Clock: New Pipe Register Error
Control Clock: Sample Register Error

aaaa is the I/O address of the Data Board:

0C2H for Data Board A Old Pipe Register,
0C4H for Data Board A New Pipe Register,
0C6H for Data Board A Sample Register,
0D2H for Data Board B Old Pipe Register,
0D4H for Data Board B New Pipe Register,
0D6H for Data Board B Sample Register,
0E2H for Data Board C Old Pipe Register,
0E4H for Data Board C New Pipe Register,
0E6H for Data Board C Sample Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 10

TITLE: RAM DATA INTEGRITY TEST

TARGET LOGIC:

6E 6D 7E 7D 8E 8D
5B 5C 6B 6C 8B 8C 9B 9C
5D 5E 9E 9D
5A 6A 8A 9A
6J 5J 5L 8J 4K
6H
All hardware in Data Path Test.

TEST DESCRIPTION:

This test performs a static test of the RAM on the Data boards. This is done using the 24 Data patterns. All 512 Memory locations are written to with the same data to the same I/O port 0C6H. Since The address counters should be advancing on each Sample Clock, all locations should be written to. This test does not check the addressing uniqueness of each location. It does verify that all Data bits are functional and totally independant of each other.

Prior to this test, the Data path up to the Old Pipe Register has been checked. There are two 10176 "D" latches between the Old Pipe Register and the RAM chip. These latches receive their clock from either WE01/ or WE02/, depending on the current Phase of the clock. The signals WE01/ and WE02 also are the write enables to the RAM chips. So The RAM chips are alternately written to on each Sample Clock.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
2	5555H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
3	AAAAH	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
4	CCCCH	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
5	3333H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
6	6666H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
7	9999H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
8	FFFFH	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
9	0001H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
10	0002H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
11	0004H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
12	0008H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
13	0010H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
14	0020H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
15	0040H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
16	0080H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
17	0100H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
18	0200H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
19	0400H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
20	0800H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
21	1000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
22	2000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
23	4000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
24	8000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
RAM Data Integrity Verify Error
Byte Count      = aaaaH
Data Read       = rrrrH
Data Expected   = eeeeH
Error Bit Map   = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the Address offset for the RAM, in the range of 0 to 1FFH.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 11

TITLE: RAM ADDRESSING INTEGRITY TEST

TARGET LOGIC:

6E 6D 7E 7D 8E 8D
5B 5C 6B 6C 8B 8C 9B 9C
5D 5E 9E 9D
5A 6A 8A 9A
6J 5J 5L 8J 4K
6H

All hardware in Data Path Test.

TEST DESCRIPTION:

This test writes a unique Data value to each of the 512 Memory locations. Each memory location should contain unique Data from each other location. The Memory is read back and each location is verified to see if each address is uniquely addressable.

The Data that is written is an incrementing pattern. The first test step starts with a value of 0001H for the first location, and the sequential locations are written to with a 0002H, 0003H, etc.

The second Test step is similar to the first, except the starting Data value is a 0002H. Subsequent test steps shift this Data value left, so that the starting Data values for the 16 test steps are:

TEST STEP INFORMATION:

Step	Start Data	Data Written to	Data Verified at
1	0001H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
2	0002H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
3	0004H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
4	0008H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
5	0010H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
6	0020H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
7	0040H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
8	0080H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
9	0100H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
10	0200H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
11	0400H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
12	0800H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
13	1000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
14	2000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
15	4000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH
16	8000H	0C6H, Diagnostic Latch	0C0H, RAM Locations 000 - 1FFH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
RAM Address Unique Error
Byte Count       = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 16.

aaaa is the Address offset for the RAM, in the range of 0 to 1FFH.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

TITLE: TRACE CONDITIONS TEST

TARGET LOGIC:

8J 8H
6H 6L 9H
12M 13M 3M 11M 10M

TRACED/ Signal P2-56 from Control Board
ARMED Signal P2-58 from Control Board

TEST DESCRIPTION:

This test uses the Control Board to provide Trace Conditions that exist on the Data Board. These are mainly "ARMED" and "TRACED/". This test is similar to the Force Conditions Test.

TEST STEP INFORMATION:

Step	Status Expected
1	45H
2	C5H
3	72H
4	71H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Trace Conditions Error
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected  = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8  = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 4.

aaaa is the I/O address of the Data Board:
0C8H for Data Board A Status Register,
0D8H for Data Board B Status Register,
0E8H for Data Board C Status Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

TITLE: RECIRCULATE RAM TEST

TARGET LOGIC:

The main hardware being tested is the feed back loop of the 10173 Multiplexers 5D, 5E, 9E and 9D, to the 10121 Multiplexers with Memory Select Enabled.

The entire Data Path and most of the Control Logic must be fuctional for this test to pass.

TEST DESCRIPTION:

The contents of the ECL RAM is recirculated out of the RAM through the Multiplexers, through the Glitch Latches, through the Sample Register, through the New Pipe Register, through the Old Pipe Register, through the RAM latch and back into the ECL RAM. All of the clocking is done by the Clock board and the Control Board.

There is a time-out counter on the recirculation, and after the recirculation is completed, the Data in the ECL RAM should be the same as before.

TEST STEP INFORMATION:

Step	Status Expected	Clock Time Out
1	8000H	10 usec
3	8000H	20 usec
5	8000H	30 usec

Step	Data Expected
2	0000H - 01FFH (incrementing pattern)
4	0000H - 01FFH (incrementing pattern)
6	0000H - 01FFH (incrementing pattern)

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

ERROR MESSAGES: (Cont'd)

Where:

ssss is the test step number in the range of 1 to 6.

hmsg is the Error heading message:

Recirculation Time out-10us clock,
Recirculation Error-10us clock,
Recirculation Time out-20us clock,
Recirculation Error-20us clock,
Recirculation Time out-30us clock,
Recirculation Error-30us clock.

aaaa is the I/O address of the Data Board:

0C0H for Data Board A RAM,
0D0H for Data Board B RAM,
0E0H for Data Board C RAM,
0F0H for Control Board Status.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE: The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

K205 CONTROL BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes the subtests that are performed by the K205 Control Board Diagnostic. The target hardware is presented, as well as a general description of each subtest, a list of information for each test step, and a dsecription of Error Messages that may be printed for the subtest results.

The Control Board Diagnostic is divided into 12 subtests, each of which is described individually on the following pages.

Subtest 1 is a Force Conditions test, subtest 2 is an Advance RAM Forward and Jump RAM backward test, subtest 3 and 4 are Detection RAMs Data and Address integrity test, subtest 5 and 6 are Delay Control RAM Data and Address integrity test, subtest 7 and 8 are Delay RAMs Data and Address integrity test, subtest 9 is Delay Counter test, subtest 10 is Relation Logic test, subtest 11 and 12 are Selection RAMs data and Address integrity test.

Subtests 1, 2, and 3 require Data Boards A, B, and C installed in the system.

The external signals through mother board to the Data Boards are checked by subtest 1, the external signals through connector J1 to the Clock Board are checked by subtest 2.

NOTE: The 'TARGET LOGIC' listed in each subtest description does not necessarily include all of the logic which could affect the operation of the subtest.

SUBTEST CATEGORY

1. Force Condition Test
2. Advance and Jump RAM Test
3. Detection RAMs Data Integrity Test
4. Detection RAMs Address Integrity Test
5. Delay Control RAM Data Integrity Test
6. Delay Control Ram Address Integrity Test
7. Delay RAMs Data Integrity Test
8. Delay RAMs Address Integrity Test
9. Delay Counter Test
10. Relation Logic Test
11. Selection RAMss Data Integrity Test
12. Selection RAMs Address Integrity Test

ERROR COUNT CATEGORY

1. Subtest 1 Error Count
2. Subtest 2 Error Count
3. Subtest 3 Error Count
4. Subtest 4 Error Count
5. Subtest 5 Error Count
6. Subtest 6 Error Count
7. Subtest 7 Error Count
8. Subtest 8 Error Count
9. Subtest 9 Error Count
10. Subtest 10 Error Count
11. Subtest 11 Error Count
12. Subtest 12 Error Count

Control Board Diagnostic Subtest 1

TITLE: FORCE CONDITION TEST

TARGET LOGIC: 6A, 7A, 5A, 4A, 11A, 5F, 7D, 5C, 5D, 7C, 4D, 8D, 1C, 3C, 8C, 9C, 5G, 11G, 4J, 12C, 14B, 12A, 12F, and 5K, 8J, 8H, 6H of DATA BOARD A, B, and C

TEST DESCRIPTION:

The force condition is functionally tested by forcing the desired condition true; the condition is then verified by reading back the corresponding status bit.

There are seven force condition tests included. Condition 0 is force level 0. Condition 1 is force jump and jump not. Condition 2 is force trace and trace not. Condition 3 is force stop and stop not. Condition 4 is force event and advance. Condition 5 is force stopped and armed. Condition 6 is force manual manual advance.

Conditon 2 also verifies the 'TRACED' signal can propagate through the mother board to data boards A, B, and C. Condition 5 also verifies the 'MEM. ARMED' signal can propagate through the mother board to data boards A, B, and C.

TEST STEP INFORMATION:

Test Step	Condition Tested	Signals in schematics
1	force level 0	'FORCE LEVEL=0'
2	force jump and jump not	'FORCE JUMP','FORCE JUMP/'
3	force trace and trace not	'FORCE TRACE','FORCE TRACE/'
4.	force stop and stop not	'FORCE STOP','FORCE STOP/'
5.	force event and advance	'FORCE EVENT AND ADVANCE'
6.	force stopped and armed	'CYCLE RESET'
7.	force manual advance	'ENABLE MANUAL ADVANCE'

ERROR MESSAGES:

1. If error condition 0 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force Level 0
Level Expected = eeH
Level Read     = rrH
```

Where zz should be 01

ee should be 00 through 0F

rr should be 00 through 0F

2. If error condition 1 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force JUMP & JUMP NOT
Jump Expected = e
Jump Read     = r
```

Where zz should be 02

e should be 0 or 1

r should be 0 or 1

3. If error condition 2 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force TRACE & TRACE NOT
Trace Expected        = e
Trace Read            = r
Old Traced A Expected = a
Old Traced A Read     = t
Old Traced B Expected = b
Old Traced B Read     = u
Old Traced C Expected = c
Old Traced C Read     = v
```

Where zz should be 03

e, r, a, t, b, u, c, v should be 0 or 1

4. If error condition 3 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force STOP & STOP NOT
Stop Expected = e
Stop Read     = r
```

Where zz should be 04

e should be 0 or 1

r should be 0 or 1

5. If error condition 4 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force EVENT & ADVANCE
Event Expected   = e
Event Read       = r
Advance Expected = p
Advance Read     = d
```

Where zz should be 05

e, r, p, d should be 0 or 1

6. If error condition 5 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force STOPPED & ARMED
Stopped Expected      = e
Stopped/ Read         = r
Armed Expected        = p
Armed/ Read           = d
Mem. Armed A Expected = a
Mem. Armed A Read     = t
Mem. Armed B Expected = b
Mem. Armed B Read     = u
Mem. Armed C Expected = c
Mem. Armed C Read     = v
```

Where zz should be 06

e, r, p, d, a, t, b, u, c, v should be 0 or 1

7. If error condition 6 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force MANUAL ADVANCE
Advance Expected        = e
AdvancE Read            = r
Manual Advance Expected = p
Man. Advance Read       = d
```

Where zz should be 07

e, r, p, d should be 0 or 1

Control Board Diagnostic Subtest 2

TITLE: ADVANCE AND JUMP RAM TEST

TARGET LOGIC: 5H, 5J, 5G, 11G, 12F, 11F,
and level memory logic in the clock board,
connector J1 included.

TEST DESCRIPTION:

The advance and jump RAMs are functionally tested by advancing the Advance RAM to the next level and restoring the jump RAM backward to a previous level. The RAM data is then verified by reading back the level and comparing the result to the expected level.

TEST STEP INFORMATION:

Test Step	RAM Tested	Level Tested	Expected Level
1 through 16	advance	00H through 0FH	Level tested + 1
17 through 32	jump	00H through 0FH	Level tested - 1

ERROR MESSAGE:

1. If an error of Advance RAM occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Adv. RAM Advancing Test
Adv. RAM Level at      = llH
Adv. RAM Data Expected = eeH
Adv. RAM Data Read     = rrH
Error Bit Map          = xxxxxxxxB
Ext. Level Expected    = ppH
Ext. Level Read        = qqH
Error Bit Map          = yyyyyyyyB
```

Where zz should be 01 through 16

ll should be 00 through 0F

ee should be 00 through 0F

rr should be 00 through 0F

pp should be 00 through 0F

qq should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111

yyyyyyyy should be 00000000 through 00001111

ERROR MESSAGE (Cont'd)

2. If an error of Jump RAM occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Jump RAM Advancing Test
Jump RAM Level at = llH
Jump RAM Data Expected = eeH
Jump RAM Data Read = rrH
```

Where zz should be 17 through 32

ll should be 00 through 0F

ee should be 00 through 0F

rr should be 00 through 0F

TITLE: DETECTION RAM DATA INTEGRITY TEST

TARGET LOGIC:

8G, 8F, 9G, 9F, 8D, 9D
4G, 4F, 7G, 7F, 3D, 4D, 7D
1G, 1F, 3G, 3F, 1D, 3D
2J, 6B, 5B, 4B, 7B, 8B, 1B, 2B, 3B, 8A, 9A
5D, 5C, 7C, 4D, 5F, 3C, 1C, 8C, 9C, 9B
12C, 12G, 12H

TEST DESCRIPTION:

The detection RAMs data integrity is functionally tested by writing a four bits nibble into each RAM, the RAM data is then verified by reading the (ADVANCE,JUMP,STOP,TRACE) nibble and comparing the result to the expected nibble.

The nibble patterns tested are:

1010B, 0101B, 1100B, 0011B, 0001B, 0010B, 0100B, 1000B.

The detection RAMs tested are:

8G, 8F, 9G, 9F, 4G, 4F, 7G, 7F, 1G, 1F, 3G, 3F.

TEST STEP INFORMATION:

Test Step	RAM Chip Location	Nibble Patterns
01 through 08	8G(00)	1010,0101,1100,0011,0001,0010,0100,1000
09 through 16	8F(01)	1010,0101,1100,0011,0001,0010,0100,1000
17 through 24	9G(02)	1010,0101,1100,0011,0001,0010,0100,1000
25 through 32	9F(03)	1010,0101,1100,0011,0001,0010,0100,1000
33 through 40	4G(04)	1010,0101,1100,0011,0001,0010,0100,1000
41 through 48	4F(05)	1010,0101,1100,0011,0001,0010,0100,1000
49 through 56	7G(06)	1010,0101,1100,0011,0001,0010,0100,1000
57 through 64	7F(07)	1010,0101,1100,0011,0001,0010,0100,1000
65 through 72	1G(08)	1010,0101,1100,0011,0001,0010,0100,1000
73 through 80	1F(09)	1010,0101,1100,0011,0001,0010,0100,1000
81 through 88	3G(10)	1010,0101,1100,0011,0001,0010,0100,1000
89 through 96	3F(11)	1010,0101,1100,0011,0001,0010,0100,1000

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Detection RAMs Data Integrity Test
RAM chip location      = cc
Detect Address         = ddH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read      = rrH
Error Bit Map          = xxxxxxxxB
```

Where cc should be 00 through 11

dd should be 00 through FF

nn should be 0A,05,0C,03,01,02,04,08

rr should be 00 through FF

xxxxxxxx should be 00000000 through 00001111

NOTE: AJST is the abbreviation of ADVANCE, JUMP, STOP, TRACE nibble.

TITLE: DETECTION RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 1H, 2H, 3H, 4H, 6H, 7H, 8H, 9H,
8G, 8F, 9G, 9F,
4G, 4F, 7G, 7F,
1G, 1F, 3G, 3F,

TEST DESCRIPTION:

The detection RAMs address integrity is functionally tested by clearing all locations of each RAM, then writing a 4 bits nibble(1010B) into the asserted address. The RAM address is then verified by reading the (ADVANCE, JUMP, STOP, TRACE) nibble from all locations and comparing the result to the nibble 0AH.

The detection RAMs tested are:

8G, 8F, 9G, 9F, 4G, 4F, 7G, 7F, 1G, 1F, 3G and 3F.

There are 8 address bits for each detection RAM, consisting of low nibble from levels and high nibble from sample registers of Data Boards.

TEST STEP INFORMATION:

Test Step	RAM Chip Location	Asserted Address Bit
1 through 8	8G(00)	01H,02H,04H,08H,10H,20H,40H,80H
9 through 16	8F(01)	01H,02H,04H,08H,10H,20H,40H,80H
17 through 24	9G(02)	01H,02H,04H,08H,10H,20H,40H,80H
25 through 32	9F(03)	01H,02H,04H,08H,10H,20H,40H,80H
33 through 40	4G(04)	01H,02H,04H,08H,10H,20H,40H,80H
41 through 48	4F(05)	01H,02H,04H,08H,10H,20H,40H,80H
49 through 56	7G(06)	01H,02H,04H,08H,10H,20H,40H,80H
57 through 64	7F(07)	01H,02H,04H,08H,10H,20H,40H,80H
65 through 72	1G(08)	01H,02H,04H,08H,10H,20H,40H,80H
73 through 80	1F(09)	01H,02H,04H,08H,10H,20H,40H,80H
81 through 88	3G(10)	01H,02H,04H,08H,10H,20H,40H,80H
89 through 96	3F(11)	01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Detection RAMs Address Integrity Test
RAM Chip Location     = cc
High Nibble Related to Data Board B
Address Expected      = ddH
Address Found         = ffH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read     = rrH
```

Where cc should be 00 through 11

b should be A,B,C

dd should be 00 through FF

ff should be 00 through FF

nn should be 0A,05,0C,03,01,02,04,08

rr should be 00 through FF

NOTE: AJST is the abbreviation of ADVANCE,JUMP,STOP,TRACE nibble.

TITLE: DELAY CONTROL RAM DATA INTEGRITY TEST

TARGET LOGIC: 13A, 12C, 12G, 12H

TEST DESCRIPTION:

The Delay Control RAM data integrity is functionally tested by writing a four bits nibble into the delay control RAM, the RAM data is then verified by reading the (EVENT MODE, END LEVEL, (D=1 IF JUMP)/, (D=1 IF ADVANCE)/) nibble from bit 14 of port 0FEH, 0FCH, 0FAH, 0F8H and compare the result to the nibble written.

There are 8 nibble patterns as follows:

1010B, 0101B, 1100B, 0011B, 0001B, 0010B, 0100B, 1000B

TEST STEP INFORMATION:

Test Step	Nibble Pattern	Levels
1	1010B	0 through 0FH
2	0101B	0 through 0FH
3	1100B	0 through 0FH
4	0011B	0 through 0FH
5	0001B	0 through 0FH
6	0010B	0 through 0FH
7	0100B	0 through 0FH
8	1000B	0 through 0FH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED -- Test Step  zz
Delay control RAM Data Integrity Test
RAM Address     = aaH
Nibble Expected = eeH
Nibble Read     = rrH
Error Bit Map   = xxxxxxxxB
```

Where aa should be 00 through 0F

ee should be 0A,05,0C,03,01,02,04,08

rr should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111

Control Board Diagnostic Subtest 6

TITLE: DELAY CONTROL RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 13A, 12C, 12G, 12H

TEST DESCRIPTION:

The Delay Control RAM address integrity is functionally tested by writing a four bits nibble (1010B) into the asserted address. The address is then verified by reading nibble data from all 16 locations,and comparing the result to the nibble expected (1010B).

TEST STEP INFORMATION:

Test Step	Nibble Pattern	Asserted Address
1	1010B	0001B
2	1010B	0010B
3	1010B	0100B
4	1010B	1000B

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay control RAM Address Integrity test
Address Expected = eeH
Address Found    = ffH
Nibble Expected  = nnH
Nibble Read      = rrH
```

Where zz should be 1 through 4

ee should be 01,02,04,08

ff should be 00 through FF

nn should be 0A.

rr should be 00 through 0F

Control Board Diagnostic Subtest 7

TITLE: DELAY RAMS DATA INTEGRITY TEST

TARGET LOGIC: 14C, 14D, 14E, 14F, 13C, 13D, 13E, 13F
11C, 11B, 12D, 12E, 12G, 12H

TEST DESCRIPTION:

The Delay RAMs data integrity is functionally tested by writing a word pattern into the delay RAMs. The word data of RAMs is then loaded into the delay counter. The data integrity is then verified by reading the word data and comparing the result to the word expected.

There are 8 delay word patterns tested as follows:

AAAAH, 5555H, CCCCH, 3333H, 1111H, 2222H, 4444H, 8888H.

TEST STEP INFORMATION:

Test Step	Word Pattern Tested
1	AAAAH
2	5555H
3	CCCCH
4	3333H
5	1111H
6	2222H
7	4444H
8	8888H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay RAM Data Integrity Test
RAM Address    = aaH
Word Expected = eeeeH
Word Read      = rrrrH
Error Bit Map = xxxxxxxxxxxxxxxxB
```

Where zz should be 1 through 8.

aa should be 00 through 0F

eeee should be AAAA,5555,CCCC,3333,1111,2222,4444,8888

rrrr should be 0000 through FFFF

xxxxxxxxxxxxxxxx should be 0000000000000000 through 1111111111111111

TITLE: DELAY RAMS ADDRESS INTEGRITY TEST

TARGET LOGIC: 14C, 14D, 14E, 14F, 13C, 13D, 13E, 13F
11C, 11B, 12D, 12E, 12G, 12H

TEST DESCRIPTION:

The Delay RAMs address integrity is functionally tested by writing a word (0AAAAH) into the asserted level address. The delay RAM is then loaded into the delay counter, and the address integrity is verified by reading the delay count from all level addresses and comparing the result to the word 0AAAAH.

There are 4 address bits are tested : 0001B, 0010B, 0100B, 1000B

TEST STEP INFORMATION:

Test Step	Word Pattern Tested	Asserted Level Address
1	AAAAH	0001B
2	AAAAH	0010B
3	AAAAH	0100B
4	AAAAH	1000B

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay RAM Address Integrity Test
Address Expected = aaH
Address Found    = ffH
Word Expected    = eeeeH
Word Read        = rrrrH
```

Where zz should be 1 through 4.

aa should be 01,02,04,08

ff should be 00 through 0F

eeee should be AAAA.

rrrr should be 0000 through FFFF

TITLE: DELAY COUNTER TEST

TARGET LOGIC: 14C, 14D, 14E, 14F, 13C, 13D, 13E, 13F
11C, 11B, 12D, 12E, 12G, 12H

TEST DESCRIPTION:

The Delay Counter is functionally tested by writing a delay word into the delay RAMs and loading it into the delay counter. The counting operation is then verified by kicking clocks, reading the delay count and comparing the result to the word expected.

The counting operation is verified by the following two methods:

1. Kick clocks until delay count is equal to 0.

2. Kick a clock to increment only one count.

The delay count word patterns being tested are as follows:

8000H, 4000H, 2000H, 1000H, 0800H, 0400H, 0200H, 0100H,

0080H, 0040H, 0020H, 0010H, 0008H, 0004H, 0002H, 0001H.

TEST STEP INFORMATION:

Test Step	Word Pattern Tested	Clocks to Kick	Expected Count
1	8000H	8000H	0
2	8000H	1	8001H
3	4000H	C000H	0
4	4000H	1	4001H
5	2000H	E000H	0
6	2000H	1	2001H
7	1000H	F000H	0
8	1000H	1	1001H
9	0800H	F800H	0
10	0800H	1	0801H
11	0400H	FC00H	0
12	0400H	1	0401H
13	0200H	FE00H	0
14	0200H	1	0201H
15	0100H	FF00H	0
16	0100H	1	0101H
17	0080H	FF80H	0
18	0080H	1	0081H
19	0040H	FFC0H	0
02	0040H	1	0041H
21	0020H	FFE0H	0
22	0020H	1	0021H
23	0010H	FFF0H	0
24	0010H	1	0011H

Test Step (Cont'd)	Word Pattern Tested	Clocks to Kick	Expected Count
25	0008H	FFF8H	0
26	0008H	1	0009H
27	0004H	FFFCH	0
28	0004H	1	0005H
29	0002H	FFFEH	0
30	0002H	1	0003H
31	0001H	FFFFH	0
32	0001H	1	0002H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay Counting Operation Test
Count Pattern  = ccccH
Count Expected = eeeeH
Count Read     = rrrrH
Error Bit Map  = xxxxxxxxxxxxxxxxB
```

Where zz should be 1 through 32

cccc should be 8000, 4000, 2000, 1000, 0800, 0400
0200, 0100, 0080, 0040, 0020, 0010
0008, 0004, 0002, 0001

eeee should be 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100
0080, 0040, 0020, 0010, 0008, 0004, 0002, 0001, 0

rrrr should be 0000 through FFFF

xxxxxxxxxxxxxxxx should be 0000000000000000 through 1111111111111111

TITLE: RELATION LOGIC TEST

TARGET LOGIC: 12B, 14B, 12A, 13A, 11A, 11F, 11C, 11B, 11D, 9B, 12F

TEST DESCRIPTION:

The Relation Logic is functionally tested by making one of the logic paths true. The relation is then verified by reading the desired relation bit and comparing the result to the expected logic state.

The Boolean function of each logic path is:

```
Path 1 : P1 = (old T < D)*(advanced + jumped)*(evented)*(TC)
Path 2 : P2 = (jumped)*(D = 1 If Jumped)
Path 3 : P3 = (advanced)*(D = 1 If advanced)*(jumped /)
Path 4 : P4 = (old T = D)*(evented /)*((advanced + jumped) /)
Path 5 : P5 = (old T = D)*(evented)*((advanced + jumped) /)
Path 6 : P6 = (old T > D)*((advanced + jumped) /)
(T < D) = NOT (P1 + P2 + P3 + P4 + P5)
(T = D) = P1 + P2 + P3 + P4
(T > D) = P5 + P6
Path 0 logic means T < D true.
```

TEST STEP INFORMATION

Test Step	Logic Path	Relation True
1	0, 1	T < D then T = D
2	2	T = D
3	3	T = D
4	4, 5, 6	T = D then T > D

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
Relation Logic Path p Failed
"T < D" Expected = a
"T < D" Read     = b
"T = D" Expected = c
"T = D" Read     = d
"T > D" Expected = e
"T > D" Read     = f
```

Where zz should be 1 through 4.

a, b, c, d, e, f should be 0 or 1.

TITLE: SELECTION RAM DATA INTEGRITY TEST

TARGET LOGIC: 6B, 5B, 4B, 7B, 8B, 1B, 2B, 3B, 8A, 9A, 5C, 5D, 7C, 4D, 8D, 5F, 7D, 1C, 3C, 8C, 9C, 3D, 9B

TEST DESCRIPTION:

The Selection RAMs data integrity is functionally tested by separating al RAMs into 4 subgroups (ADVANCE, JUMP, STOP, TRACE), writing the specified data into into the RAMS of each subgroup, and verifying the data integrity by reading the (ADVANCE, JUMP, STOP, TRACE) bits and comparing the result to the nibble expected.

There are 4 subgroups as follows, being tested:

Subgroup A : bit 0 -- selection bit for ADVANCE A
bit 1 -- selection bit for ADVANCE B
bit 2 -- selection bit for ADVANCE C
bit 3 -- selection bit for (ADVANCE C.B.A)/
bit 4 -- selection bit for ADVANCE if T > D
bit 5 -- selection bit for ADVANCE if T = D
bit 6 -- selection bit for ADVANCE if T < D
bit 7 -- selection bit for ADVANCE if 'x'

Subgroup J : bit 0 -- selection bit for JUMP A
bit 1 -- selection bit for JUMP B
bit 2 -- selection bit for JUMP C
bit 3 -- selection bit for (JUMP C.B.A)/
bit 4 -- selection bit for JUMP if T > D
bit 5 -- selection bit for JUMP if T = D
bit 6 -- selection bit for JUMP if T < D

Subgroup S : bit 0 -- selection bit for STOP A
bit 1 -- selection bit for STOP B
bit 2 -- selection bit for STOP C
bit 3 -- selection bit for (STOP C.B.A)/
bit 4 -- selection bit for STOP if T > D
bit 5 -- selection bit for STOP if T = D
bit 6 -- selection bit for STOP if T < D
bit 7 -- selection bit for STOP if 'x'

Subgroup T : bit 0 -- selection bit for TRACE A
bit 1 -- selection bit for TRACE B
bit 2 -- selection bit for TRACE C
bit 3 -- selection bit for (TRACE C.B.A)/
bit 4 -- selection bit for TRACE if T > D
bit 5 -- selection bit for TRACE if T = D
bit 6 -- selection bit for TRACE if T < D
bit 7 -- selection bit for TRACE if 'x'

Each bit has logic 0 and logic 1 to be tested.

TEST STEP INFORMATION:

Test Step	Subgroup	Bit	Mnemonic	Logic State	Related Chip
1	Advance	0	ADVANCE A	0	4B-D3
2	Advance	0	ADVANCE A	1	4B-D3
3	Advance	1	ADVANCE B	0	5B-D2
4	Advance	1	ADVANCE B	1	5B-D2
5	Advance	2	ADVANCE C	0	5B-D3
6	Advance	2	ADVANCE C	1	5B-D3
7	Advance	3	(ADVANCE C.B.A)/	0	5B-D1
8	Advance	3	(ADVANCE C.B.A)/	1	5B-D1
9	Advance	4	ADVANCE if T > D	0	6B-D2
10	Advance	4	ADVANCE if T > D	1	6B-D2
11	Advance	5	ADVANCE if T = D	0	6B-D0
12	Advance	5	ADVANCE if T = D	1	6B-D0
13	Advance	6	ADVANCE if T < D	0	6B-D3
14	Advance	6	ADVANCE if T < D	1	6B-D3
15	Advance	7	ADVANCE if 'x'	0	6B-D1
16	Advance	7	ADVANCE if 'x'	1	6B-D1
17	Jump	0	Jump A	0	8B-D2
18	Jump	0	Jump A	1	8B-D2
19	Jump	1	Jump B	0	8B-D3
20	Jump	1	Jump B	1	8B-D3
21	Jump	2	Jump C	0	4B-D0
22	Jump	2	Jump C	1	4B-D0
23	Jump	3	(Jump C.B.A)/	0	4B-D2
24	Jump	3	(Jump C.B.A)/	1	4B-D2
25	Jump	4	Jump if T > D	0	7B-D3
26	Jump	4	Jump if T > D	1	7B-D3
27	Jump	5	Jump if T = D	0	7B-D1
28	Jump	5	Jump if T = D	1	7B-D1
29	Jump	6	Jump if T < D	0	7B-D2
30	Jump	6	Jump if T < D	1	7B-D2
31	Jump	7	None	x	None
32	Jump	7	None	x	None
33	Stop	0	Stop A	0	3B-D2
34	Stop	0	Stop A	1	3B-D2
35	Stop	1	Stop B	0	2B-D0
36	Stop	1	Stop B	1	2B-D0
37	Stop	2	Stop C	0	2B-D2
38	Stop	2	Stop C	1	2B-D2
39	Stop	3	(Stop C.B.A)/	0	1B-D1
40	Stop	3	(Stop C.B.A)/	1	1B-D1
41	Stop	4	Stop if T > D	0	1B-D0
42	Stop	4	Stop if T > D	1	1B-D0
43	Stop	5	Stop if T = D	0	1B-D3
44	Stop	5	Stop if T = D	1	1B-D3
45	Stop	6	Stop if T < D	0	1B-D2
46	Stop	6	Stop if T < D	1	1B-D2
47	Stop	7	Stop if 'x'	0	2B-D3
48	Stop	7	Stop if 'x'	1	2B-D3
49	Trace	0	Trace A	0	9A-D0
50	Trace	0	Trace A	1	9A-D0
51	Trace	1	Trace B	0	8A-D2
52	Trace	1	Trace B	1	8A-D2

53	Trace	2	Trace C	0	8A-D0
54	Trace	2	Trace C	1	8A-D0
55	Trace	3	(Trace C.B.A)/	0	8A-D1
56	Trace	3	(Trace C.B.A)/	1	8A-D1
57	Trace	4	Trace if T > D	0	9A-D2
58	Trace	4	Trace if T > D	1	9A-D2
59	Trace	5	Trace if T = D	0	9A-D3
60	Trace	5	Trace if T = D	1	9A-D3
61	Trace	6	Trace if T < D	0	3B-D0
62	Trace	6	Trace if T < D	1	3B-D0
63	Trace	7	Trace if'x'	0	3B-D1
64	Trace	7	Trace if'x'	1	3B-D1

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Selection RAMs Data Integrity
Subgroup g Bit b Testing
RAM Address           = aaH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read     = rrH
Error Bit Map         = xxxxxxxxB
```

Where zz should be 1 through 64

g should be A, J, S, T.

b should be 0 or 1.

aa should be 00 through 0F.

nn should be 08, 04, 02, 01, 0

rr should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111

Control Board Diagnostic Subtest 12

TITLE: SELECTION RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 6B, 5B, 4B, 7B, 8B, 1B, 2B, 3B, 8A, 9A, 5C, 5D, 7C, 4D, 8D, 5F, 7D, 1C, 3C, 8C, 9C, 3D, 9B

TEST DESCRIPTION:

The Selection RAMs address integrity is functionally tested by separating all RAMs into 4 subgroups (ADVANCE, JUMP, STOP, TRACE), clearing all locations of selection RAMs, going to the asserted level address, and writing bit 0 into the RAMS of each subgroup. The address integrity is then verified by reading the (ADVANCE, JUMP, STOP, TRACE) bits from all locations.

There are 4 subgroups as follows, being tested:

Subgroup A : bit 0 -- selection bit for ADVANCE A
Subgroup J : bit 0 -- selection bit for JUMP A
Subgroup S : bit 0 -- selection bit for STOP A
Subgroup T : bit 0 -- selection bit for TRACE A

Each bit only test logic 0.

TEST STEP INFORMATION:

Test Step	Subgroup	Bit	Mnemonic	Logic State	Level Address
1	Advance	0	ADVANCE A	0	01H
2	Advance	0	ADVANCE A	0	02H
3	Advance	0	ADVANCE A	0	04H
4	Advance	0	ADVANCE A	0	08H
5	Jump	0	JUMP A	0	01H
6	Jump	0	JUMP A	0	02H
7	Jump	0	JUMP A	0	04H
8	Jump	0	JUMP A	0	08H
9	Stop	0	STOP A	0	01H
10	Stop	0	STOP A	0	02H
11	Stop	0	STOP A	0	04H
12	Stop	0	STOP A	0	08H
13	TRACE	0	TRACE A	0	01H
14	TRACE	0	TRACE A	0	02H
15	TRACE	0	TRACE A	0	04H
16	TRACE	0	TRACE A	0	08H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Selection RAMs Address Integrity
Subgroup g Testing
Address Expected      = eeH
Address Found         = ffH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read     = rrH
```

Where zz should be 1 through 16

g should be A, J, S, T.

ee should be 01, 02, 04, 08

ff should be 00 through 0F

nn should be 08, 04, 02, 01

rr should be 00 through 0F

K205 CLOCK BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes subtests that are performed by the K205 Clock Board Diagnostic. The target hardware is presented, as well as a general description of each Subtest, a list of information for each Test Step, and Error Messages that may be printed.

The K205 Clock Board Diagnostic is a board level Diagnostic which runs under the K205 Diagnostic Operating System. The Diagnostic verifies all functions of the Clock Board except for "J2", which presents clocks to the front panel. The hardware that is not tested is a 4028 Multiplexer/Driver at 9B, two drivers at 10B, and the cable going to the front panel.

The Diagnostic Tests that are performed can be divided into five basic sections as described below.

The first is the Force Conditions Test. This test is a series of simple I/O operations that are performed on the Clock Board.

The second is the Sample and Control Clock testing. These clocks move data on the Data Boards. Specifically, the Sample Clock clocks the Data Board's Sample Registers, and the Control Clock clocks the Data Board's Pipeline.

The third is the Latch Clock testing. The Latch Clocks also clock data on the Data Boards, but in a special "latch mode" where data is latched before it reaches the Data Board's Sample Registers.

The fourth is the Frequency testing. All seven decades from the 100Mhz Clock, down to the 100 Hz Clock are tested. The Clock Board Multiplier is tested to see if it can actually perform a divide by function, thus slowing down the clock rate.

The fifth and final is the testing of the Level RAM. The RAM is tested for Data integrity, Addressing integrity, and control logic functionality.

The Diagnostic uses Data Boards A, B and C extensively to check out the clocking features. The Diagnostic also requires the use of the Control Board and the Threshold Board. All of these boards must be functional for any realistic pinpointing of possible failures. All six of the external probes must be installed, with floating inputs (no connection).

If Data Board C is not installed, (i.e. unit contains 32 input channels), the C section clocks of the Clock Board will not be tested, and the following message is displayed:

>Testing sections A & B, cannot test section C.

This message informs the operator that the A and B sections are being tested, but there is insufficient hardware in the system to diagnose section C. All six probes must still be installed to properly test sections A and B.

The type of tests that are performed on the Clock Board are static type tests. The tests verify the functionality and individuality of multiplexers and gates but do not perform "real time" testing on the board. Therefore, if racing conditions exist, or if problems occur with propagation delays, the Diagnostic will probably not detect them.

Also, the frequency test that is performed on the Clock Decades is a "ballpark" test, and does not verify that the 100 Mhz source clock is exactly 100.00 Mhz. This must be adjusted/verified with a scope or frequency counter.

The Clock Board provides very little status information to monitor the Modes or selections. Of the 133 Command Output Bits, the Clock board only provides 4 Status Input Bits.

If multiple failures exist on a board under test, the problem might originate in the I/O port decoding and data latching. This portion of the board is initially assumed to be functional. If it is not funtional, very few if any tests will pass.

DESCRIPTION OF DATA BOARD REGISTERS USED TO TEST CLOCK BOARD

The Sample Clocks, Latch Clocks and Control Clocks are tested using the K205 Data Boards. The Data Boards are also used for the Frequency tests.

A simple outline of the registers on the Data Boards is as follows:

1. Data Boards Diagnostic Latch Register.

   Data Board A - Write Port 0C0H. (cannot read this port back)
   Data Board B - Write Port 0D0H. (cannot read this port back)
   Data Board C - Write Port 0E0H. (cannot read this port back)

   This Latch is the "Front End" to the Data Board's Data Path. Data is placed in this register by simply performing an OUTWORD instruction.

2. Data Boards Sample Registers.

   Data Board A - Read Port 0C6H. (cannot write directly to this port)
   Data Board B - Read Port 0D6H. (cannot write directly to this port)
   Data Board C - Read Port 0D6H. (cannot write directly to this port)

   Data is transfered from the Data Board's Diagnostic Latch Registers to the Data Board's Sample Register when a Sample Clock is issued. Sample Register A requires Sample Clock A, Sample Register B requires Sample Clock B, and Sample Register C requires Sample Clock C. This transfer will take place assuming the Data Board is not in "Latch" mode.

3. Data Boards New Pipe Registers.

   Data Board A - Read Port 0C4H. (cannot write directly to this port)
   Data Board B - Read Port 0D4H. (cannot write directly to this port)
   Data Board C - Read Port 0D4H. (cannot write directly to this port)

Data is transferred from the Data Boards Sample Registers to the Data Boards New Pipe Registers when a Control Clock is issued. Data Boards A, B and C all use a single Control Clock for transfer.

4. "Latch" Mode on the Data Boards.

When the Data Boards are in Latch Mode, an extra Data latch is present between the Diagnostic Latch Registers and the Sample Registers. A Latch Clock is required to transfer Data.

In Latch Mode, the following sequence is required to place Data into the Data Board's Sample Registers.

Output the desired Data to the Diagnostic Latch Registers. This will present the Data to the input of the "Latch" mode Registers. Issuing a Latch Clock presents this Data to the input of the Sample Registers. Issuing a Sample Clock latches this Data in the Sample Registers. Data Board A requires Latch Clock A, Data Board B requires Latch Clock B, and Data Board C requires Latch Clock C.

SUBTEST CATEGORIES

There are fourteen subtests that are performed by the Clock Board Diagnostic. These tests are as follows:

1. Force Conditions Test
2. Sample and Control Clocks, Diagnostic Internal Clock Test
3. Sample and Control Clocks, OR-only Enables Test
4. Sample Clocks, 10ns Clock Test
5. Sample and Control Clocks, AJ, BJ and CJ Clocks Test
6. Sample and Control Clocks, AK, BK and CK Clocks Test
7. Latch Clocks, Diagnostic Internal Clock Test
8. Latch Clocks, Diagnostic OR-only Enables Test
9. Latch Clocks, AR, BR and CR Clocks Test
10. Latch Clocks, AS, BS and CS Clocks Test
11. Decade Frequency and Multiplier Divide by Test
12. Level RAMs Data Integrity Test
13. Level RAMs Address Integrity Test
14. Level RAMs Control Test

ERROR COUNT CATEGORIES

The Error Count Display information is a one for one match with the subtest above. The K205 Diagnostic Operating System will display the message "Subtest n" instead of the actual test name (where "n" = Subtest Number).

Subtest 1 (Force Conditions)
Subtest 2 (Sample and Control Clocks, Diagnostic Internal)
Subtest 3 (Sample and Control Clocks, OR-only Enables)
Subtest 4 (Sample Clocks, 10ns Clock Test
Subtest 5 (Sample and Control Clocks, AJ, BJ and CJ)
Subtest 6 (Sample and Control Clocks, AK, BK and CK)

Subtest 7	(Latch Clocks, Diagnostic Internal)
Subtest 8	(Latch Clocks, Diagnostic OR-only Enables)
Subtest 9	(Latch Clocks, AR, BR and CR)
Subtest 10	(Latch Clocks, AS, BS and CS)
Subtest 11	(Decade Frequency and Multiplier)
Subtest 12	(Level RAMs Data Integrity)
Subtest 13	(Level RAMs Address Integrity)
Subtest 14	(Level RAMs Control)

TITLE: FORCE CONDITIONS TEST

TARGET LOGIC: 7J, 6J, 8J, 10K,
11K, 12J, 6K, 9K, 9J, 11H
10H
10G, 10F, 9F, 11K,
5J

TEST DESCRIPTION:

This test issues commands to the Clock Board and expects to see certain status conditions existing. Commands are issued by writing to port 0BEH, and the Status is read back from port 0B2H.

Since the Clock Board only provides 4 status bits for all of the 113 command bits, only a fraction of the I/O read/write/control logic is actually tested. If there are errors in this test, the I/O decode logic and/or data latches may be faulty, and the succeeding tests will probably have multiple errors.

TEST STEP INFORMATION:

Step	Expected Status
1	A000H
2	2000H
3	0000H
4	6000H, 7000H
5	7000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Force Conditions/Status Error
No Clocking used
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range of 1 to 5.

aaaa is the address of the Clock Board Status Register, 00B2H.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Status Register.

NOTE: With the limited amount of status bits on the Clock Board, it is difficult to pin point the cause of an error. Whether the fault lies with an address decoder, a Data Bit Driver or Latch, the fault can be determined objectively by using a Logic Analyzer or Scope, and setting the Loop On Error Option.

Clock Board Diagnostic Subtest 2

TITLE: SAMPLE AND CONTROL CLOCKS, DIAGNOSTIC INTERNAL CLOCK TEST

TARGET LOGIC:

7A, 8A, 10H, 7B, 8B, 9G
7D, 8D, 10J, 7E, 8E, 9H
7F, 8F, 7G, 8G, 7H, 8H
11H, 10D, 12C, 11C
10C
11B
3E, 3F, 3G, 3H, 4H, 4J, 4C, 4D

TEST DESCRIPTION:

The Diagnostic Internal Sample Clocks A, B and C, and the Diagnostic Internal Control Clock will be tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing a Diagnostic Internal Sample Clock, and checking the Sample Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing a Diagnostic Internal Control Clock, and checking the New Pipe Registers to see if a Data transfer took place.

NOTE: The Diagnostic Internal Clock is "kicked" by outputing a "1" to bit D0 of Write Registers 0B8H of the Clock Board. This produces a clock pulse the width of the 8086's Write pulse. Consecutive "kicks" can be achieved by consecutive outputs to this port. It is never necessary to set this bit low.

TEST STEP INFORMATION:

Step	Data	Clock Tested	Data Verified at
1	0000H	Sample A, B, C	Sample Registers A, B, C
2	5555H	Sample A, B, C	Sample Registers A, B, C
3	AAAAH	Sample A, B, C	Sample Registers A, B, C
4	CCCCH	Sample A, B, C	Sample Registers A, B, C
5	3333H	Sample A, B, C	Sample Registers A, B, C
6	6666H	Sample A, B, C	Sample Registers A, B, C
7	9999H	Sample A, B, C	Sample Registers A, B, C
8	FFFFH	Sample A, B, C	Sample Registers A, B, C
9	0000H	Control	New Pipe Registers A, B, C
10	5555H	Control	New Pipe Registers A, B, C
11	AAAAH	Control	New Pipe Registers A, B, C
12	CCCCH	Control	New Pipe Registers A, B, C
13	3333H	Control	New Pipe Registers A, B, C
14	6666H	Control	New Pipe Registers A, B, C
15	9999H	Control	New Pipe Registers A, B, C
16	FFFFH	Control	New Pipe Registers A, B, C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
17	AAAAH	0000H	0000H	Sample A	Sample Registers A, B, C
18	0000H	BBBBH	0000H	Sample B	Sample Registers A, B, C
19	0000H	0000H	CCCCH	Sample C	Sample Registers A, B, C
20	AAAAH	BBBBH	CCCCH	Control	Sample Registers A, B, C
21	AAAAH	BBBBH	CCCCH	Control	Sample Registers A, B, C
22	AAAAH	BBBBH	CCCCH	Control	Sample Registers A, B, C
23	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C
24	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C
25	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C

NOTE: Test Steps 20 - 22 verify the Control Clock does not change the contents of the Sample Registers.

Test Steps 23 - 25 verify the Control Clock can latch Data into the New Pipe Pipe Registers with all Sample Clocks disabled.

Disable Test

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
26	AAAAH	-----	-----	Sample A	Sample Register A
27	-----	BBBBH	-----	Sample B	Sample Register B
28	-----	-----	CCCCH	Sample C	Sample Register C
29	0000H	-----	-----	Control	New Pipe Register A
30	-----	0000H	-----	Control	New Pipe Register B
31	-----	-----	0000H	Control	New Pipe Register C

Force Disqualify Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
32	AAAAH	-----	-----	Sample A	Sample Register A
33	-----	BBBBH	-----	Sample B	Sample Register B
34	-----	-----	CCCCH	Sample C	Sample Register C
35	0000H	-----	-----	Control	New Pipe Register A
36	-----	0000H	-----	Control	New Pipe Register B
37	-----	-----	0000H	Control	New Pipe Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
Diagnostic Internal Clock
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 37.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify

aaaa is the address of a Data Board Sample Register:
0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.
or a Data Board New Pipe Register:
0C4H for Data Board A,
0D4H for Data Board B,
0E4H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
0000H,
5555H,
AAAAH,
CCCCH,
3333H,
6666H,
9999H,
FFFFH.

NOTE: 0000H is the expected Data Word for Data Boards during Uniqueness Testing.

TITLE: SAMPLE AND CONTROL CLOCKS OR-ONLY ENABLES TEST

TARGET LOGIC: 5E, 5F, 5G, 5H, 4H, 4J, 4C, 4D

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Sample Clocks A, B and C, and Control Clock's OR-Only Enable bits are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Force Disqualify Disable test.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing a Sample Clock by toggling the OR-Only Enable bit, and checking the Sample Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing a Control Clock by toggling the OR-Only Enable bit, and checking the New Pipe Registers to see if a Data transfer took place.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A	Sample Register A
2	BBBBH	Sample B	Sample Register B
3	CCCCH	Sample C	Sample Register C
4	AAAAH	Control	New Pipe Register A
5	BBBBH	Control	New Pipe Register B
6	CCCCH	Control	New Pipe Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Sample A	Sample Registers A, B, C
8	0000H	BBBBH	0000H	Sample B	Sample Registers A, B, C
9	0000H	0000H	CCCCH	Sample C	Sample Registers A, B, C
10	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C
11	AAAAH	BBBBH	CCCCH	Control	New Pipe Registers A, B, C

Force Disqualify Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
12	AAAAH	-----	-----	Sample A	Sample Register A
13	-----	BBBBH	-----	Sample B	Sample Register B
14	-----	-----	CCCCH	Sample C	Sample Register C
15	0000H	-----	-----	Control	New Pipe Register A
16	-----	0000H	-----	Control	New Pipe Register B
17	-----	-----	0000H	Control	New Pipe Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
OR Only Enables
I/O Address     = aaaaH
Status Read     = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 17.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Force Disqualify.

aaaa is the address of a Data Board Sample Register:
0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.
or a Data Board New Pipe Register:
0C4H for Data Board A,
0D4H for Data Board B,
0E4H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
AAAAH for Data Board A, (0C6H, 0C4H).
BBBBH for Data Board B, (0D6H, 0D4H).
CCCCH for Data Board C, (0E6H, 0E4H).

NOTE: 0000H is the expected data word for all Data Boards during Uniqueness Testing.

TITLE: SAMPLE CLOCKS, 10ns CLOCK TEST

TARGET LOGIC: 5E, 5F, 5G, 4H, 4J, 4C, 4D

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Sample Clocks A, B, C, and 10ns Clock Enable bit will be tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, toggling the 10ns Enable bit, and then checking the Sample Registers to see if a Data transfer took place.

NOTE: The 10ns Enable bit is toggled active then inactive with two consecutive output instructions by the 8086 CPU. Since the 100Mhz Clock is so fast compared to the execution speed of the 8086, many Sample Clocks will occur during the short period that the 10ns Enable is active. This will not cause a problem, since the Sample Register cannot overflow.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A	Sample Register A
2	BBBBH	Sample B	Sample Register B
3	CCCCH	Sample C	Sample Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
4	AAAAH	0000H	0000H	Sample A	Sample Registers A, B, C
5	0000H	BBBBH	0000H	Sample B	Sample Registers A, B, C
6	0000H	0000H	CCCCH	Sample C	Sample Registers A, B, C

Force Disqualify Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	-----	-----	Sample A	Sample Register A
8	-----	BBBBH	-----	Sample B	Sample Register B
9	-----	-----	CCCCH	Sample C	Sample Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
10 ns Clock
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 9.

cccc is the tested Clock: Sample A,
Sample B,
Sample C.

tttt is the test type: Functional,
Uniqueness,
Force Disqualify.

aaaa is the address of a Data Board Sample Register:
0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

NOTE: 0000H is the expected Data Word for all Data Boards during Testing.

TITLE: SAMPLE AND CONTROL CLOCKS AJ, BJ, and CJ CLOCKS TEST

TARGET LOGIC: 3E, 5E, 3F, 5F, 3G, 5G, 3H, 5H
4H, 4J, 4C, 4D
4E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AJ, AJ/, BJ, BJ/, CJ and CJ/ clock enables for the Sample Clocks A, B, C and the Control Clock will be tested for functionality and uniqueness as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing a Sample Clock by toggling one of the AJ, BJ, CJ Enables, and checking the Sample Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing a Control Clock by toggling one of the AJ, BJ, CJ Enables, and checking the New Pipe Registers to see if a Data transfer took place.

NOTE: The Logic states of AJ, AJ/, BJ, BJ/, CJ and CJ/ are determined by the current threshold at the probes. An ECL Threshold, and a VARAIABLE A Threshold will be used to provide the High and Low logic states. This test will require the use of the Threshold Board and the probes.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A - AJ/, BJ/, CJ/	Sample Register A
2	BBBBH	Sample B - AJ/, BJ/, CJ/	Sample Register B
3	CCCCH	Sample C - AJ/, BJ/, CJ/	Sample Register C
4	AAAAH	Control - AJ/, BJ/, CJ/	New Pipe Register A
5	BBBBH	Control - AJ/, BJ/, CJ/	New Pipe Register B
6	CCCCH	Control - AJ/, BJ/, CJ/	New Pipe Register C
7	AAAAH	Sample A - AJ, BJ, CJ	Sample Register A
8	BBBBH	Sample B - AJ, BJ, CJ	Sample Register B
9	CCCCH	Sample C - AJ, BJ, CJ	Sample Register C
10	AAAAH	Control - AJ, BJ, CJ	New Pipe Register A
11	BBBBH	Control - AJ, BJ, CJ	New Pipe Register B
12	CCCCH	Control - AJ, BJ, CJ	New Pipe Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
13	AAAAH	0000H	0000H	Sample A - AJ/	Sample Registers A, B, C
14	AAAAH	0000H	0000H	Sample A - BJ/	Sample Registers A, B, C
15	AAAAH	0000H	0000H	Sample A - CJ/	Sample Registers A, B, C
16	0000H	BBBBH	0000H	Sample B - AJ/	Sample Registers A, B, C
17	0000H	BBBBH	0000H	Sample B - BJ/	Sample Registers A, B, C
18	0000H	BBBBH	0000H	Sample B - CJ/	Sample Registers A, B, C
19	0000H	0000H	CCCCH	Sample C - AJ/	Sample Registers A, B, C
20	0000H	0000H	CCCCH	Sample C - BJ/	Sample Registers A, B, C
21	0000H	0000H	CCCCH	Sample C - CJ/	Sample Registers A, B, C
22	AAAAH	BBBBH	CCCCH	Control - AJ/	New Pipe Registers A, B, C
23	AAAAH	BBBBH	CCCCH	Control - BJ/	New Pipe Registers A, B, C
24	AAAAH	BBBBH	CCCCH	Control - CJ/	New Pipe Registers A, B, C
25	AAAAH	0000H	0000H	Sample A - AJ	Sample Registers A, B, C
26	AAAAH	0000H	0000H	Sample A - BJ	Sample Registers A, B, C
27	AAAAH	0000H	0000H	Sample A - CJ	Sample Registers A, B, C
28	0000H	BBBBH	0000H	Sample B - AJ	Sample Registers A, B, C
29	0000H	BBBBH	0000H	Sample B - BJ	Sample Registers A, B, C
30	0000H	BBBBH	0000H	Sample B - CJ	Sample Registers A, B, C
31	0000H	0000H	CCCCH	Sample C - AJ	Sample Registers A, B, C
32	0000H	0000H	CCCCH	Sample C - BJ	Sample Registers A, B, C
33	0000H	0000H	CCCCH	Sample C - CJ	Sample Registers A, B, C
34	AAAAH	BBBBH	CCCCH	Control - AJ	New Pipe Registers A, B, C
35	AAAAH	BBBBH	CCCCH	Control - BJ	New Pipe Registers A, B, C
36	AAAAH	BBBBH	CCCCH	Control - CJ	New Pipe Registers A, B, C

Threshold Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
37	AAAAH	BBBBH	CCCCH	Sample A - AJ/	Sample Registers A, B, C
38	AAAAH	BBBBH	CCCCH	Sample A - BJ/	Sample Registers A, B, C
39	AAAAH	BBBBH	CCCCH	Sample A - CJ/	Sample Registers A, B, C
40	AAAAH	BBBBH	CCCCH	Sample B - AJ/	Sample Registers A, B, C
41	AAAAH	BBBBH	CCCCH	Sample B - BJ/	Sample Registers A, B, C
42	AAAAH	BBBBH	CCCCH	Sample B - CJ/	Sample Registers A, B, C
43	AAAAH	BBBBH	CCCCH	Sample C - AJ/	Sample Registers A, B, C
44	AAAAH	BBBBH	CCCCH	Sample C - BJ/	Sample Registers A, B, C
45	AAAAH	BBBBH	CCCCH	Sample C - CJ/	Sample Registers A, B, C
46	0000H	0000H	0000H	Control - AJ/	New Pipe Registers A, B, C
47	0000H	0000H	0000H	Control - BJ/	New Pipe Registers A, B, C
48	0000H	0000H	0000H	Control - CJ/	New Pipe Registers A, B, C
49	AAAAH	BBBBH	CCCCH	Sample A - AJ	Sample Registers A, B, C
50	AAAAH	BBBBH	CCCCH	Sample A - BJ	Sample Registers A, B, C
51	AAAAH	BBBBH	CCCCH	Sample A - CJ	Sample Registers A, B, C
52	AAAAH	BBBBH	CCCCH	Sample B - AJ	Sample Registers A, B, C
53	AAAAH	BBBBH	CCCCH	Sample B - BJ	Sample Registers A, B, C
54	AAAAH	BBBBH	CCCCH	Sample B - CJ	Sample Registers A, B, C
55	AAAAH	BBBBH	CCCCH	Sample C - AJ	Sample Registers A, B, C
56	AAAAH	BBBBH	CCCCH	Sample C - BJ	Sample Registers A, B, C
57	AAAAH	BBBBH	CCCCH	Sample C - CJ	Sample Registers A, B, C
58	0000H	0000H	0000H	Control - AJ	New Pipe Registers A, B, C
59	0000H	0000H	0000H	Control - BJ	New Pipe Registers A, B, C
60	0000H	0000H	0000H	Control - CJ	New Pipe Registers A,B,C

Force Disqualify Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
61	AAAAH	BBBBH	CCCCH	Sample A - AJ/	Sample Registers A, B, C
62	AAAAH	BBBBH	CCCCH	Sample A - BJ/	Sample Registers A, B, C
63	AAAAH	BBBBH	CCCCH	Sample A - CJ/	Sample Registers A, B, C
64	AAAAH	BBBBH	CCCCH	Sample B - AJ/	Sample Registers A, B, C
65	AAAAH	BBBBH	CCCCH	Sample B - BJ/	Sample Registers A, B, C
66	AAAAH	BBBBH	CCCCH	Sample B - CJ/	Sample Registers A, B, C
67	AAAAH	BBBBH	CCCCH	Sample C - AJ/	Sample Registers A, B, C
68	AAAAH	BBBBH	CCCCH	Sample C - BJ/	Sample Registers A, B, C
69	AAAAH	BBBBH	CCCCH	Sample C - CJ/	Sample Registers A, B, C
70	0000H	0000H	0000H	Control - AJ/	New Pipe Registers A, B, C
71	0000H	0000H	0000H	Control - BJ/	New Pipe Registers A, B, C
72	0000H	0000H	0000H	Control - CJ/	New Pipe Registers A, B, C
73	AAAAH	BBBBH	CCCCH	Sample A - AJ	Sample Registers A, B, C
74	AAAAH	BBBBH	CCCCH	Sample A - BJ	Sample Registers A, B, C
75	AAAAH	BBBBH	CCCCH	Sample A - CJ	Sample Registers A, B, C
76	AAAAH	BBBBH	CCCCH	Sample B - AJ	Sample Registers A, B, C
77	AAAAH	BBBBH	CCCCH	Sample B - BJ	Sample Registers A, B, C
78	AAAAH	BBBBH	CCCCH	Sample B - CJ	Sample Registers A, B, C
79	AAAAH	BBBBH	CCCCH	Sample C - AJ	Sample Registers A, B, C
80	AAAAH	BBBBH	CCCCH	Sample C - BJ	Sample Registers A, B, C
81	AAAAH	BBBBH	CCCCH	Sample C - CJ	Sample Registers A, B, C
82	0000H	0000H	0000H	Control - AJ	New Pipe Registers A, B, C
83	0000H	0000H	0000H	Control - BJ	New Pipe Registers A, B, C
84	0000H	0000H	0000H	Control - CJ	New Pipe Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 84.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify.

qqqq is the tested Clock Enable: AJ/ BJ/ CJ/,
AJ BJ CJ,
AJ/,
BJ/,
CJ/,
AJ,
BJ,
CJ.

aaaa is the address of a Data Board Sample Register:
0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.
or a Data Board New Pipe Register:
0C4H for Data Board A,
0D4H for Data Board B,
0E4H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
AAAAH for Data Board A, (0C6H, 0C4H).
BBBBH for Data Board B, (0D6H, 0D4H).
CCCCH for Data Board C, (0E6H, 0E4H).

NOTE: 0000H is the expected Data Word for all Data Boards during Uniqueness Testing.

TITLE: SAMPLE AND CONTROL CLOCKS AK, BK AND CK CLOCKS TEST

TARGET LOGIC: 5A, 4A, 5B, 5C, 5D, 4C, 4D,
5E, 5F, 5G, 5H, 4H, 4J,
6A

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AK, AK/, BK, BK/, CK and CK/ clock enables for the Sample Clocks A, B, C, and the Control Clock will be tested for functionality and uniqueness, as well as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing a Sample Clock by toggling one of the AK, BK, CK Enables, and checking the Sample Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing a Control Clock by toggling one of the AK, BK, CK Enables, and checking the New Pipe Registers to see if a Data transfer took place.

NOTE: The Logic states of AK, AK/, BK, BK/, CK and CK/ are determined by the current threshold at the probes. An ECL Threshold, and a VARAIABLE A Threshold will be used to provide the High and Low logic states.

This test will require the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A - AK/, BK/, CK/	Sample Register A
2	BBBBH	Sample B - AK/, BK/, CK/	Sample Register B
3	CCCCH	Sample C - AK/, BK/, CK/	Sample Register C
4	AAAAH	Control - AK/, BK/, CK/	New Pipe Register A
5	BBBBH	Control - AK/, BK/, CK/	New Pipe Register B
6	CCCCH	Control - AK/, BK/, CK/	New Pipe Register C
7	AAAAH	Sample A - AK, BK, CK	Sample Register A
8	BBBBH	Sample B - AK, BK, CK	Sample Register B
9	CCCCH	Sample C - AK, BK, CK	Sample Register C
10	AAAAH	Control - AK, BK, CK	New Pipe Register A
11	BBBBH	Control - AK, BK, CK	New Pipe Register B
12	CCCCH	Control - AK, BK, CK	New Pipe Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
13	AAAAH	0000H	0000H	Sample A - AK/	Sample Registers A, B, C
14	AAAAH	0000H	0000H	Sample A - BK/	Sample Registers A, B, C
15	AAAAH	0000H	0000H	Sample A - CK/	Sample Registers A, B, C
16	0000H	BBBBH	0000H	Sample B - AK/	Sample Registers A, B, C
17	0000H	BBBBH	0000H	Sample B - BK/	Sample Registers A, B, C
18	0000H	BBBBH	0000H	Sample B - CK/	Sample Registers A, B, C
19	0000H	0000H	CCCCH	Sample C - AK/	Sample Registers A, B, C
20	0000H	0000H	CCCCH	Sample C - BK/	Sample Registers A, B, C
21	0000H	0000H	CCCCH	Sample C - CK/	Sample Registers A, B, C
22	AAAAH	BBBBH	CCCCH	Control - AK/	New Pipe Registers A, B, C
23	AAAAH	BBBBH	CCCCH	Control - BK/	New Pipe Registers A, B, C
24	AAAAH	BBBBH	CCCCH	Control - CK/	New Pipe Registers A, B, C
25	AAAAH	0000H	0000H	Sample A - AK	Sample Registers A, B, C
26	AAAAH	0000H	0000H	Sample A - BK	Sample Registers A, B, C
27	AAAAH	0000H	0000H	Sample A - CK	Sample Registers A, B, C
28	0000H	BBBBH	0000H	Sample B - AK	Sample Registers A, B, C
29	0000H	BBBBH	0000H	Sample B - BK	Sample Registers A, B, C
30	0000H	BBBBH	0000H	Sample B - CK	Sample Registers A, B, C
31	0000H	0000H	CCCCH	Sample C - AK	Sample Registers A, B, C
32	0000H	0000H	CCCCH	Sample C - BK	Sample Registers A, B, C
33	0000H	0000H	CCCCH	Sample C - CK	Sample Registers A, B, C
34	AAAAH	BBBBH	CCCCH	Control - AK	New Pipe Registers A, B, C
35	AAAAH	BBBBH	CCCCH	Control - BK	New Pipe Registers A, B, C
36	AAAAH	BBBBH	CCCCH	Control - CK	New Pipe Registers A, B, C

Threshold Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
37	AAAAH	BBBBH	CCCCH	Sample A - AK/	Sample Registers A, B, C
38	AAAAH	BBBBH	CCCCH	Sample A - BK/	Sample Registers A, B, C
39	AAAAH	BBBBH	CCCCH	Sample A - CK/	Sample Registers A, B, C
40	AAAAH	BBBBH	CCCCH	Sample B - AK/	Sample Registers A, B, C
41	AAAAH	BBBBH	CCCCH	Sample B - BK/	Sample Registers A, B, C
42	AAAAH	BBBBH	CCCCH	Sample B - CK/	Sample Registers A, B, C
43	AAAAH	BBBBH	CCCCH	Sample C - AK/	Sample Registers A, B, C
44	AAAAH	BBBBH	CCCCH	Sample C - BK/	Sample Registers A, B, C
45	AAAAH	BBBBH	CCCCH	Sample C - CK/	Sample Registers A, B, C
46	0000H	0000H	0000H	Control - AK/	New Pipe Registers A, B, C
47	0000H	0000H	0000H	Control - BK/	New Pipe Registers A, B, C
48	0000H	0000H	0000H	Control - CK/	New Pipe Registers A, B, C
49	AAAAH	BBBBH	CCCCH	Sample A - AK	Sample Registers A, B, C
50	AAAAH	BBBBH	CCCCH	Sample A - BK	Sample Registers A, B, C
51	AAAAH	BBBBH	CCCCH	Sample A - CK	Sample Registers A, B, C
52	AAAAH	BBBBH	CCCCH	Sample B - AK	Sample Registers A, B, C
53	AAAAH	BBBBH	CCCCH	Sample B - BK	Sample Registers A, B, C
54	AAAAH	BBBBH	CCCCH	Sample B - CK	Sample Registers A, B, C
55	AAAAH	BBBBH	CCCCH	Sample C - AK	Sample Registers A, B, C
56	AAAAH	BBBBH	CCCCH	Sample C - BK	Sample Registers A, B, C
57	AAAAH	BBBBH	CCCCH	Sample C - CK	Sample Registers A, B, C
58	0000H	0000H	0000H	Control - AK	New Pipe Registers A, B, C
59	0000H	0000H	0000H	Control - BK	New Pipe Registers A, B, C
60	0000H	0000H	0000H	Control - CK	New Pipe Registers A, B, C

Force Disqualify Test

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
61	AAAAH	BBBBH	CCCCH	Sample A - AK/	Sample Registers A, B, C
62	AAAAH	BBBBH	CCCCH	Sample A - BK/	Sample Registers A, B, C
63	AAAAH	BBBBH	CCCCH	Sample A - CK/	Sample Registers A, B, C
64	AAAAH	BBBBH	CCCCH	Sample B - AK/	Sample Registers A, B, C
65	AAAAH	BBBBH	CCCCH	Sample B - BK/	Sample Registers A, B, C
66	AAAAH	BBBBH	CCCCH	Sample B - CK/	Sample Registers A, B, C
67	AAAAH	BBBBH	CCCCH	Sample C - AK/	Sample Registers A, B, C
68	AAAAH	BBBBH	CCCCH	Sample C - BK/	Sample Registers A, B, C
69	AAAAH	BBBBH	CCCCH	Sample C - CK/	Sample Registers A, B, C
70	0000H	0000H	0000H	Control - AK/	New Pipe Registers A, B, C
71	0000H	0000H	0000H	Control - BK/	New Pipe Registers A, B, C
72	0000H	0000H	0000H	Control - CK/	New Pipe Registers A, B, C
73	AAAAH	BBBBH	CCCCH	Sample A - AK	Sample Registers A, B, C
74	AAAAH	BBBBH	CCCCH	Sample A - BK	Sample Registers A, B, C
75	AAAAH	BBBBH	CCCCH	Sample A - CK	Sample Registers A, B, C
76	AAAAH	BBBBH	CCCCH	Sample B - AK	Sample Registers A, B, C
77	AAAAH	BBBBH	CCCCH	Sample B - BK	Sample Registers A, B, C
78	AAAAH	BBBBH	CCCCH	Sample B - CK	Sample Registers A, B, C
79	AAAAH	BBBBH	CCCCH	Sample C - AK	Sample Registers A, B, C
80	AAAAH	BBBBH	CCCCH	Sample C - BK	Sample Registers A, B, C
81	AAAAH	BBBBH	CCCCH	Sample C - CK	Sample Registers A, B, C
82	0000H	0000H	0000H	Control - AK	New Pipe Registers A, B, C
83	0000H	0000H	0000H	Control - BK	New Pipe Registers A, B, C
84	0000H	0000H	0000H	Control - CK	New Pipe Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected  = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 84.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify

qqqq is the tested Clock Enable: AK/ BK/ CK/,
AK BK CK,
AK/,
BK/,
CK/,
AK,
BK,
CK

aaaa is the address of a Data Board Sample Register:
0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.
or a Data Board New Pipe Register:
0C4H for Data Board A,
0D4H for Data Board B,
0E4H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
AAAAH for Data Board A, (0C6H, 0C4H).
BBBBH for Data Board B, (0D6H, 0D4H).
CCCCH for Data Board C, (0E6H, 0E4H).

NOTE: 0000H is the expected Data Word for all Data Boards during Uniqueness Testing.

TITLE: LATCH CLOCKS, DIAGNOSTIC INTERNAL CLOCK TEST

TARGET LOGIC: 11H, 1F, 1G, 1H, 2H
1D, 2B, 2A, 2C, 2D
6A

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Diagnostic Internal Latch Clocks A, B and C are tested for functionality as well as the ability to disable these Clocks using the Normal Disable and the Latch Disqualify Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, issuing a Diagnostic Latch Clock, issuing a Diagnostic Sample Clock, and checking the Sample Registers to see if a Data transfer took place.

NOTE: The Diagnostic Latch Clock is "kicked" by outputing a "1" to bit D1 of Write Register 0B8H of the Clock Board. This produces a clock pulse the width of the 8086's Write pulse. Consecutive "kicks" can be achieved by consecutive outputs to this port. It is never necessary to set this bit low.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	0000H	Latch A, B, C	Sample Registers A, B, C
2	5555H	Latch A, B, C	Sample Registers A, B, C
3	AAAAH	Latch A, B, C	Sample Registers A, B, C
4	CCCCH	Latch A, B, C	Sample Registers A, B, C
5	3333H	Latch A, B, C	Sample Registers A, B, C
6	6666H	Latch A, B, C	Sample Registers A, B, C
7	9999H	Latch A, B, C	Sample Registers A, B, C
8	FFFFH	Latch A, B, C	Sample Registers A, B, C

Threshold Disable Test:

Step	Data	Clock Tested	Data Verified at
9	AAAAH	Latch A	Sample Register A
10	BBBBH	Latch B	Sample Register B
11	CCCCH	Latch C	Sample Register C

Latch Disqualify Disable Test:

Step	Data	Clock Tested	Data Verified at
12	AAAAH	Latch A	Sample Register A
13	BBBBH	Latch B	Sample Register B
14	CCCCH	Latch C	Sample Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
Diagnostic Latch Clock
I/O Address     = aaaaH
Status Read     = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 14.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Threshold Disable,
Disqualify Disable.

aaaa is the address of a Data Board Sample Register:
0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
Data for Functional Testing:
0000H,
5555H,
AAAAH,
CCCCH,
3333H,
6666H,
9999H,
FFFFH.
Data for Threshold Disable and Disqualify Disable Testing:
AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

Clock Board Diagnostic Subtest 8

TITLE: LATCH CLOCKS, OR-ONLY ENABLES TEST

TARGET LOGIC: 2E, 2F, 2G, 2H
1D, 2B, 2A, 2C, 2D

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Latch Clocks A, B and C OR-Only Enables are tested for functionality, and the ability to disable these Clocks using the the Latch Disqualify Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, issuing a Diagnostic Latch Clock, issuing a Diagnostic Sample Clock, and checking the Sample Registers to see if a Data transfer took place.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A	Sample Register A
2	BBBBH	Latch B	Sample Register B
3	CCCCH	Latch C	Sample Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
4	AAAAH	0000H	0000H	Latch A	Sample Registers A, B, C
5	0000H	BBBBH	0000H	Latch B	Sample Registers A, B, C
6	0000H	0000H	CCCCH	Latch C	Sample Registers A, B, C

Latch Disqualify Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	BBBBH	CCCCH	Latch A	Sample Registers A, B, C
8	AAAAH	BBBBH	CCCCH	Latch B	Sample Registers A, B, C
9	AAAAH	BBBBH	CCCCH	Latch C	Sample Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
OR Only Enables
I/O Address     = aaaaH
Status Read     = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 9.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Uniqueness,
Latch Disqualify Disable.

aaaa is the address of a Data Board Sample Register:
0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

NOTE: 0000H is the expected data word for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 9

TITLE: LATCH CLOCKS, AR, BR AND CR CLOCKS TEST

TARGET LOGIC: 1F, 2E, 1G, 2F, 1H, 2G, 2H
1D, 2B, 2A, 2C, 2D
1E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AR, AR/, BR, BR/, CR and CR/ Clock Enables for Latch Clocks A, B, and C are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable, and the Latch Disqualify Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, issuing a Latch Clock by toggling one of the AR, BR, CR Enables, and issuing a Diagnostic Internal Sample Clock and checking the Sample Registers to see if a Data transfer took place.

NOTE: The Logic states of AR, AR/, BR, BR/, CR and CR/ are determined by the current threshold at the probes. An ECL Threshold, and a VARIABLE A Threshold will be used to provide the High and Low logic states.

This test requires the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A - AR/, BR/, CR/	Sample Register A
2	BBBBH	Latch B - AR/, BR/, CR/	Sample Register B
3	CCCCH	Latch C - AR/, BR/, CR/	Sample Register C
4	AAAAH	Latch A - AR, BR, CR	Sample Register A
5	BBBBH	Latch B - AR, BR, CR	Sample Register B
6	CCCCH	Latch C - AR, BR, CR	Sample Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Latch A - AR/	Sample Registers A, B, C
8	AAAAH	0000H	0000H	Latch A - BR/	Sample Registers A, B, C
9	AAAAH	0000H	0000H	Latch A - CR/	Sample Registers A, B, C
10	0000H	BBBBH	0000H	Latch B - AR/	Sample Registers A, B, C
11	0000H	BBBBH	0000H	Latch B - BR/	Sample Registers A, B, C
12	0000H	BBBBH	0000H	Latch B - CR/	Sample Registers A, B, C
13	0000H	0000H	CCCCH	Latch C - AR/	Sample Registers A, B, C

14	0000H	0000H	CCCCH	Latch C - BR/	Sample Registers A, B, C
15	0000H	0000H	CCCCH	Latch C - CR/	Sample Registers A, B, C
16	AAAAH	0000H	0000H	Latch A - AR	Sample Registers A, B, C
17	AAAAH	0000H	0000H	Latch A - BR	Sample Registers A, B, C
18	AAAAH	0000H	0000H	Latch A - CR	Sample Registers A, B, C
19	0000H	BBBBH	0000H	Latch B - AR	Sample Registers A, B, C
20	0000H	BBBBH	0000H	Latch B - BR	Sample Registers A, B, C
21	0000H	BBBBH	0000H	Latch B - CR	Sample Registers A, B, C
22	0000H	0000H	CCCCH	Latch C - AR	Sample Registers A, B, C
23	0000H	0000H	CCCCH	Latch C - BR	Sample Registers A, B, C
24	0000H	0000H	CCCCH	Latch C - CR	Sample Registers A, B, C

Threshold Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
25	AAAAH	BBBBH	CCCCH	Latch A - AR/	Sample Registers A, B, C
26	AAAAH	BBBBH	CCCCH	Latch A - BR/	Sample Registers A, B, C
27	AAAAH	BBBBH	CCCCH	Latch A - CR/	Sample Registers A, B, C
28	AAAAH	BBBBH	CCCCH	Latch B - AR/	Sample Registers A, B, C
29	AAAAH	BBBBH	CCCCH	Latch B - BR/	Sample Registers A, B, C
30	AAAAH	BBBBH	CCCCH	Latch B - CR/	Sample Registers A, B, C
31	AAAAH	BBBBH	CCCCH	Latch C - AR/	Sample Registers A, B, C
32	AAAAH	BBBBH	CCCCH	Latch C - BR/	Sample Registers A, B, C
33	AAAAH	BBBBH	CCCCH	Latch C - CR/	Sample Registers A, B, C
34	AAAAH	BBBBH	CCCCH	Latch A - AR	Sample Registers A, B, C
35	AAAAH	BBBBH	CCCCH	Latch A - BR	Sample Registers A, B, C
36	AAAAH	BBBBH	CCCCH	Latch A - CR	Sample Registers A, B, C
37	AAAAH	BBBBH	CCCCH	Latch B - AR	Sample Registers A, B, C
38	AAAAH	BBBBH	CCCCH	Latch B - BR	Sample Registers A, B, C
39	AAAAH	BBBBH	CCCCH	Latch B - CR	Sample Registers A, B, C
40	AAAAH	BBBBH	CCCCH	Latch C - AR	Sample Registers A, B, C
41	AAAAH	BBBBH	CCCCH	Latch C - BR	Sample Registers A, B, C
42	AAAAH	BBBBH	CCCCH	Latch C - CR	Sample Registers A, B, C

Latch Disqualify Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
43	AAAAH	BBBBH	CCCCH	Latch A - AR/	Sample Registers A, B, C
44	AAAAH	BBBBH	CCCCH	Latch A - BR/	Sample Registers A, B, C
45	AAAAH	BBBBH	CCCCH	Latch A - CR/	Sample Registers A, B, C
46	AAAAH	BBBBH	CCCCH	Latch B - AR/	Sample Registers A, B, C
47	AAAAH	BBBBH	CCCCH	Latch B - BR/	Sample Registers A, B, C
48	AAAAH	BBBBH	CCCCH	Latch B - CR/	Sample Registers A, B, C
49	AAAAH	BBBBH	CCCCH	Latch C - AR/	Sample Registers A, B, C
50	AAAAH	BBBBH	CCCCH	Latch C - BR/	Sample Registers A, B, C
51	AAAAH	BBBBH	CCCCH	Latch C - CR/	Sample Registers A, B, C
52	AAAAH	BBBBH	CCCCH	Latch A - AR	Sample Registers A, B, C
53	AAAAH	BBBBH	CCCCH	Latch A - BR	Sample Registers A, B, C
54	AAAAH	BBBBH	CCCCH	Latch A - CR	Sample Registers A, B, C
55	AAAAH	BBBBH	CCCCH	Latch B - AR	Sample Registers A, B, C
56	AAAAH	BBBBH	CCCCH	Latch B - BR	Sample Registers A, B, C
57	AAAAH	BBBBH	CCCCH	Latch B - CR	Sample Registers A, B, C
58	AAAAH	BBBBH	CCCCH	Latch C - AR	Sample Registers A, B, C
59	AAAAH	BBBBH	CCCCH	Latch C - BR	Sample Registers A, B, C
60	AAAAH	BBBBH	CCCCH	Latch C - CR	Sample Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enable
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 60.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Uniqueness,
Threshold Disable,
Latch Disqualify Disable.

qqqq is the tested Clock Enable: AR/ BR/ CR/,
AR BR CR,
AR/,
BR/,
CR/,
AR,
BR,
CR.

aaaa is the address of a Data Board Sample Register:
0C6H for Data Board A,
0D6H for Data Board B,
0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
AAAAH for Data Board A.
BBBBH for Data Board B.
CCCCH for Data Board C.

NOTE: 0000H is the expected data word for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 10

TITLE: LATCH CLOCKS AS, BS AND CS CLOCKS TEST

TARGET LOGIC: 2B, 2A, 2C, 2D, 1D, 2E, 2F, 2G, 2H
3A

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AS, AS/, BS, BS/, CS and CS/ Clock Enables for Latch Clocks A, B and C are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, asserting the appropriate AS, BS, CS Enables, issuing a Diagnostic Latch Clock, and issuing a Diagnostic Internal Sample Clock and checking the Sample Registers to see if a Data transfer took place.

NOTE 1: This test is different than the rest due to the transparent mode of the 10130 Latches on the Data Boards. When the Latch Clock is held in a low state, the 10130 Latches on the Data Board are transparent, i.e., the "Q" output follows the "D" input. When the Latch Clock goes high, this latches the Data into the 10130's and the "D" input then becomes a don't care.

In this test, instead of toggling the enable to the AS, BS or CS, it is held active and a Diagnostic Int Clock issued. This causes the Data Board to be in Latch Mode, instead of being transparent.

NOTE 2: The Logic states of AR, AR/, BR, BR/, CR and CR/ are determined by the current threshold at the probes. An ECL Threshold, and a VARIABLE A Threshold are used to provide the High and Low logic states.

This test requires the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality Test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A - AS/, BS/, CS/	Sample Register A
2	BBBBH	Latch B - AS/, BS/, CS/	Sample Register B
3	CCCCH	Latch C - AS/, BS/, CS/	Sample Register C
4	AAAAH	Latch A - AS, BS, CS	Sample Register A
5	BBBBH	Latch B - AS, BS, CS	Sample Register B
6	CCCCH	Latch C - AS, BS, CS	Sample Register C

Uniqueness Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Latch A - AS/	Sample Registers A, B, C
8	AAAAH	0000H	0000H	Latch A - BS/	Sample Registers A, B, C
9	AAAAH	0000H	0000H	Latch A - CS/	Sample Registers A, B, C
10	0000H	BBBBH	0000H	Latch B - AS/	Sample Registers A, B, C
11	0000H	BBBBH	0000H	Latch B - BS/	Sample Registers A, B, C
12	0000H	BBBBH	0000H	Latch B - CS/	Sample Registers A, B, C
13	0000H	0000H	CCCCH	Latch C - AS/	Sample Registers A, B, C
14	0000H	0000H	CCCCH	Latch C - BS/	Sample Registers A, B, C
15	0000H	0000H	CCCCH	Latch C - CS/	Sample Registers A, B, C
16	AAAAH	0000H	0000H	Latch A - AS	Sample Registers A, B, C
17	AAAAH	0000H	0000H	Latch A - BS	Sample Registers A, B, C
18	AAAAH	0000H	0000H	Latch A - CS	Sample Registers A, B, C
19	0000H	BBBBH	0000H	Latch B - AS	Sample Registers A, B, C
20	0000H	BBBBH	0000H	Latch B - BS	Sample Registers A, B, C
21	0000H	BBBBH	0000H	Latch B - CS	Sample Registers A, B, C
22	0000H	0000H	CCCCH	Latch C - AS	Sample Registers A, B, C
23	0000H	0000H	CCCCH	Latch C - BS	Sample Registers A, B, C
24	0000H	0000H	CCCCH	Latch C - CS	Sample Registers A, B, C

Threshold Disable Test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
25	AAAAH	BBBBH	CCCCH	Latch A - AS/	Sample Registers A, B, C
26	AAAAH	BBBBH	CCCCH	Latch A - BS/	Sample Registers A, B, C
27	AAAAH	BBBBH	CCCCH	Latch A - CS/	Sample Registers A, B, C
28	AAAAH	BBBBH	CCCCH	Latch B - AS/	Sample Registers A, B, C
29	AAAAH	BBBBH	CCCCH	Latch B - BS/	Sample Registers A, B, C
30	AAAAH	BBBBH	CCCCH	Latch B - CS/	Sample Registers A, B, C
31	AAAAH	BBBBH	CCCCH	Latch C - AS/	Sample Registers A, B, C
32	AAAAH	BBBBH	CCCCH	Latch C - BS/	Sample Registers A, B, C
33	AAAAH	BBBBH	CCCCH	Latch C - CS/	Sample Registers A, B, C
34	AAAAH	BBBBH	CCCCH	Latch A - AS	Sample Registers A, B, C
35	AAAAH	BBBBH	CCCCH	Latch A - BS	Sample Registers A, B, C
36	AAAAH	BBBBH	CCCCH	Latch A - CS	Sample Registers A, B, C
37	AAAAH	BBBBH	CCCCH	Latch B - AS	Sample Registers A, B, C
38	AAAAH	BBBBH	CCCCH	Latch B - BS	Sample Registers A, B, C
39	AAAAH	BBBBH	CCCCH	Latch B - CS	Sample Registers A, B, C
40	AAAAH	BBBBH	CCCCH	Latch C - AS	Sample Registers A, B, C
41	AAAAH	BBBBH	CCCCH	Latch C - BS	Sample Registers A, B, C
42	AAAAH	BBBBH	CCCCH	Latch C - CS	Sample Registers A, B, C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enable
I/O Address      = aaaaH
```

```
        Status Read     = rrrrH
        Status Expected = eeeeH

Where:
ssss is the Test Step in the range: 1 to 42.

cccc is the tested Clock: Latch A,
                          Latch B,
                          Latch C.

tttt is the test type:  Functional,
                        Uniqueness,
                        Threshold Disable.

qqqq is the tested Clock Enable: AS/ BS/ CS/,
                                 AS BS CS,
                                 AS/,
                                 BS/,
                                 CS/,
                                 AS,
                                 BS,
                                 CS.

aaaa is the address of a Data Board Sample Register:
                        0C6H for Data Board A,
                        0D6H for Data Board B,
                        0E6H for Data Board C.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Sample Register which should be:
                        AAAAH for Data Board A.
                        BBBBH for Data Board B.
                        CCCCH for Data Board C.

NOTE:  0000H is the expected data word for all Data Boards during
Uniqueness Testing.
```

Clock Board Diagnostic Subtest 11

TITLE: DECADE FREQUENCY AND MULTIPLIER DIVIDE BY TEST

TARGET LOGIC: 10D, 12C, 11C
10C
11B
9E, 10E, 9C, 9D

Setup Latches in Subtest 2

100Mhz Oscilator Descrete Componets (Grid 8B-6B)

TEST DESCRIPTION:

This test will check the Clock Decade multiplexer, (Decade), and the divide by counter, (Multiplier).

The 100Mhz, 10Mhz, 1Mhz, 100Khz, 10Khz, 1Khz and 100hz Clocks will be tested with various Multipliers. The Clock frequencies will be verified within a ballpark range, but this will only verify that the multiplexer is selecting different Decades. A frequency counter is required to adjust/verify the Time Period of the 100Mhz Clock.

When the faster Clock frequencies are being tested, the testing time is very quick, and the following message will be displayed:

>Counting Clock Pulses...

During the 1Khz test, (this one takes a while), the following message will be displayed:

>Counting Clock Pulses... 4 seconds

During the 100hz test, (this one takes a long time), the following message will be displayed:

>Counting Clock Pulses...20 seconds

During the testing of the Multiplier Divide by counter, the following message will be displayed:

>Checking the Multiplier Divide by...

TEST STEP INFORMATION:

Decade Frequency Test:

Step	Decade	Mult	Clks Expected	Clks Minimum	Clks Maximum
1	0	8	256	128	384
2	1	8	256	128	384
3	2	8	256	128	384
4	3	8	256	128	384
5	4	8	256	128	384
6	5	8	256	128	384
7	6	8	256	128	384

Multiplier Divide by Test:

Step	Decade	Mult	Clks Expected	Clks Minimum	Clks Maximum
8	3	0	~83	0	512
9	3	1	~89	Step 8 Clock Count	512
10	3	2	~95	Step 9 Clock Count	512
11	3	3	~97	Step 10 Clock Count	512
12	3	4	~111	Step 11 Clock Count	512
13	3	5	~122	Step 12 Clock Count	512
14	3	6	~134	Step 13 Clock Count	512
15	3	7	~148	Step 14 Clock Count	512
16	3	8	~167	Step 15 Clock Count	512
17	3	9	~191	Step 16 Clock Count	512
18	3	10	~224	Step 17 Clock Count	512
19	3	11	~270	Step 18 Clock Count	512
20	3	12	~336	Step 19 Clock Count	512
21	3	13	~450	Step 20 Clock Count	512
22 *	3	14	256	0	512
23 *	3	15	256	0	512

NOTE 1: The values above preceeded by ~ are aproximate values. They were selected by running the test a single time on a single K205. This value will vary from System to System due to minor differences in the CPU's Clock frequency, and other hardware propagation times. The precise values are not important as long as Clock count increments while the Multiplier incrementes.

NOTE 2: Test Steps 22 and 23 are different from the rest. When the Multiplier goes from 13 to 14, and from 14 to 15, the Clock count no longer follows the slow-linear increase that it followed with the Multiplier range of 0 to 12. The Clock count aproximately doubles, so a ballparking method of 256 clocks inside the 0 to 512 range is used.

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg Error
Decade x:  ffff Clock
Multiplier       = mmmmD
Clocks counted   = ccccD
Min Clock count = llllD
Max Clock count = hhhhD
```

Where:
ssss is the Test Step in the range: 1 to 23.

hmsg is "Clock Frequency Counting",
"Multiplier Clock Divide by".

x is the selected Decade: 0, 1, 2, 3, 4, 5, 6.

ffff is the Clock frequency:

100	Mhz,
10	Mhz,
1	Mhz,
100	Khz,
10	Khz,
1	Khz,
100	hz.

mmmm is the current Multiplier value, range is 0 to 15.

cccc is the Number of clocks counted, range is 0 to 512.

llll is the Minimum number of clocks that could be counted for frequency.

hhhh is the Maximum number of clocks that could be counted for frequency.

Clock Board Diagnostic Subtest 12

TITLE: LEVEL RAMs DATA INTEGRITY TEST

TARGET LOGIC: 11E, 11F
11J
12F, 12G
12D, 10D, 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Level RAMs on the Clock Board are organized as 512 x 4. They are written to by the Control Board, and read into the highest nibble of the word from port B0H of the Clock Board.

The Level RAM's Data Integrity is checked by writing all 16 possible values to the RAM, and reading it back to verify that each Data Bit is functional and unique.

TEST STEP INFORMATION:

Data Integrity Test:

Step	Data	Address Locations
1	0000H	000 - 511
2	0001H	000 - 511
3	0002H	000 - 511
4	0003H	000 - 511
5	0004H	000 - 511
6	0005H	000 - 511
7	0006H	000 - 511
8	0007H	000 - 511
9	0008H	000 - 511
10	0009H	000 - 511
11	000AH	000 - 511
12	000BH	000 - 511
13	000CH	000 - 511
14	000DH	000 - 511
15	000EH	000 - 511
16	000FH	000 - 511

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Level RAM Data Integrity Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 16.

cccc is RAM byte count, (address) in the range of 0 to 511.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

Clock Board Diagnostic Subtest 13

TITLE: LEVEL RAMs ADDRESS INTEGRITY TEST

TARGET LOGIC:
11D
11G, 12H
11E, 11F
11J
12F, 12G
12D, 10D, 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Level RAMs address is provided by dual counters which provide eight address lines which can address 256 locations. An additions flip flop toggles back and forth between the two 10422 RAM Chips on each Write/Read, to allow the access of 512 RAM locations.

The Level RAMs are tested for addressing uniqueness. This will verify that each of 512 locations can be written to independently of all other locations.

TEST STEP INFORMATION:

Step 1. An incrementing Data pattern from 00H to 0FH is written to RAM, which repeats after each 16 locations. This verifies address lines A0, A1, A2 and A3.

Step 2. A Block Incrementing Data pattern from 00H to 0FH is written to RAM, which repeats after each 256 locations. This verifies address lines A4, A5, A6 and A7.

Step 3. A Block Data pattern of 05H and 0AH is written to RAM, which covers all 512 locations. This verifies that both of the 10422 RAM chips are written to.

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Level RAM Address Uniqueness Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 3.

cccc is RAM byte count, (address) in the range of 0 to 511.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

TITLE: LEVEL RAMs CONTROL TEST

TARGET LOGIC:
11D
11G, 12H
11E, 11F
11J
12F, 12G
12D, 10D, 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

This Subtest verifies the functionality of the Control Logic associated with the Level RAM.

The First Test Step checks the odd/even toggling of the level ram. Each Consecutive write operation to the RAM should toggle back and forth between the "Even 10422" RAM chip, and the "ODD 10422" RAM chip. A "D" latch is acting as a flip flop, and providing a write enable signal to only one RAM chip. An 0AH will be written to all Even addresses and a 05H to all Odd.

The Second Test Step checks the Level RAM Write Enable/Disable function. The Level RAM is Write enabled when the signals 'ARMED' and 'TRACED' from the Control Board are both active.

This test does 7 writes with the following conditions:

LEVEL	ARMED	TRACED	RESULT
0	1	1	0
1	1	1	1
2	1	0	not recorded
3	1	0	not recorded
4	1	1	4
5	1	1	5
5	0	1	not recorded

The Third Test Step checks the Recirculation feature of the Level RAM. The Data is read out of the 10422 RAM chips, looped back, and written back in. This is checked by writing an incrementing pattern into the RAM, and then reading it back, verifying the Data Integrity.

The Data is then read back a second time and verified. On the second read, the Data will be shifted by one Address location from the Recirculation.

The Fourth Test Step checks the Level RAM reset persistence by first filling the RAM with a value of 00H, then holding the reset line to the RAM address counters active, and hammering address location 0 by performing 512 consecutive write operations. This should modify the Data Value at location 0, but the other 511 locations should be unchanged. All 512 locations are read back and verified.

TEST STEP INFORMATION:

Step	Data Even Locations	Data Odd Locations
1	000AH	0005H

Step	Data	Address	
2	0000H	000	
	0001H	001	
	0004H	002	
	0005H	003	
Step	Data	Address	
4	0005H	000	(0005H in Location 000 Only)
	0000H	001	
	0000H	002	
	.	.	
	.	.	
	0000H	510	
	0000H	511	

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 4.

hmsg is Level RAM odd/even Toggle,
Level RAM Write enable/disable,
Level RAM Recirculation,
Level RAM Hammer/Addr Reset.

cccc is RAM byte count, (address) in the range of 0 to 511.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

Odd/Even Test:

0005H,
000AH.

Write Disable/Enable Test:

0000H,
0001H,
0004H,
0005H.

Recirculation Test:

0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

Hammer/Address Reset Test:

0005H,
0000H.

K205 LOGIC ANALYZER THRESHOLD/GPIB/RS-232 BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes the subtests executed on the K205 Threshold/ GPIB/RS-232 Board, how Error Reporting is accomplished, and the concept behind each subtest program.

The Threshold/GPIB/RS-232 board diagnostics is divided into nine subtests, each of which is described individually on the following pages.

Subtest 1 is a DAC 7541 linearity test; subtest 2 is a DAC 7533 linearity test; subtest 3 is a Multiplexer/threshold test, subtest 4 is a serial I/O #1 test; subtest 5 is a serial I/O #2 test, subtest 6 is a 8253 counter mode 1 test; subtest 7 through subtest 9 are GPIB internal logic tests (the GPIB cable and operator intervene flag should not be set); subtest 7 is GPIB control status test; subtest 8 is GPIB MPU interrupt logic test; subtest 9 is GPIB data out register and parallel poll response register test.

Subtests 4 and 5 require a RS-232 wrap back connector installed to perform the test.

Only a part of the GPIB logic is checked in the GPIB internal test (i.e. subtests 7 through 9 check internal logic only); external handshake logic is not tested.

NOTE: The 'TARGET LOGIC' listed in each subtest description does not necessarily include all of the logic which could affect the operation of the subtest.

SUBTEST CATEGORY

1. DAC 7541 LINEARITY TEST
2. DAC 7533 LINEARITY TEST
3. MUX/THRESHOLD LOGIC TEST
4. SERIAL I/O #1 TEST
5. SERIAL I/O #2 TEST
6. TIMER 8253 COUNTER 0 TEST
7. GPIB INTERNAL CONTROL LINE TEST
8. GPIB INTERNAL MPU INTERRUPT LOGIC TEST
9. GPIB INTERNAL DATA REGISTER TEST

ERROR COUNT CATEGORY

1. SUBTEST 1 ERROR COUNT.
2. SUBTEST 2 ERROR COUNT.
3. SUBTEST 3 ERROR COUNT.
4. SUBTEST 4 ERROR COUNT.
5. SUBTEST 5 ERROR COUNT.
6. SUBTEST 6 ERROR COUNT.
7. SUBTEST 7 ERROR COUNT.
8. SUBTEST 8 ERROR COUNT.
9. SUBTEST 9 ERROR COUNT.

TITLE: DAC 7541 LINEARITY TEST

TARGET LOGIC: 5E, 6E, 8B, 7F, 8F, 8A
7A, 7E, Q2
and power supply +5.0V, -5.2V, -2.0V, AGND, -10.0V, +10.0V,
VBB(+3.0V), +15V(divided as +7.5V), -15V(divided as -7.5V)

TEST DESCRIPTION:

The DAC 7541 linearity is functionally tested by using the +10.0V, -10.0V, AGND, -2.0V, -5.2V, +5.0V, +3.0V, +7.5V, -7.5V, +0.00V, +1.30V and -1.40V as reference voltage, multiplexed through 7F as noninverting input, and writing data into 8A as inverting input until Q2 toggles its state. The ADC status is then verified by reading port 04H bit 0.

When the reference voltage is +10.0V, the DAC 7541 is initially programmed to -10.0V, so Q2 is turned on. The ADC status bit is equal to 0 which increments the DAC 7541 output voltage until the ADC status bit toggles its state.

When the reference voltages are -10.0V, AGND, -2.0V, -5.2V, +5.0V, +3.0V, +7.50V, -7.50V, DVM input, +1.30V, and -1.40V, the DAC 7541 is initially programmed to +10.0V, so Q2 is turned off. The ADC status bit is equal to 1, decrementing the DAC 7541 output voltage until the ADC status bit toggles its state.

TEST STEP INFORMATION:

Step	Reference Voltage	Initial 7541 Data Voltage	Initial ADC Status
1	+10.0V	0FFFH (-10.0V)	0
2	-10.0V	0000H (+10.0V)	1
3	AGND	0000H (+10.0V)	1
4	-2.0V	0000H (+10.0V)	1
5	-5.2V	0000H (+10.0V)	1
6	+5.0V	0000H (+10.0V)	1
7	VBB(+3.0V)	0000H (+10.0V)	1
8	+15V/2	0000H (+10.0V)	1
9	-15V/2	0000H (+10.0V)	1
10	DVM	0000H (+10.0V)	1
11	-ECL	0000H (+10.0V)	1
12	+TTL	0000H (+10.0V)	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
DAC 7541 Linearity Test
Voltage Expected     = see.eee
Voltage Lower Limit = suu.uuu
Voltage Upper Limit = sll.lll
Actual Voltage Read = saa.aaa
ADC Status Expected = x
ADC Status Expected = y
```

Where zz should be in the range of 1 through 12

s should be + or -

ee.eee should be in the range of 00.000 through 10.000

uu.uuu should be 9.940, 10.235, 0.300, 2.350, 5.625, 4.820
2.700, 7.380, 7.980, 0.300, 1.000, 1.700

ll.lll should be 10.240, 9.935, 0.300, 1.750, 5.025, 5.420
3.300, 7.980, 7.380, 0.300, 1.600, 1.100

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1

TITLE: DAC 7533 LINEARITY TEST

TARGET LOGIC: 6D, 4B, 12B, 9B, 9A, 4A, 5A, 10A, 6F, 7A, 8A, Q2, 8F, 5E, 6E, 8B

TEST DESCRIPTION:

The DAC 7533 linearity is functionally tested by using the DAC 7541 as reference voltage. VAR A and VAR B are multiplexed through 6F as the noninverting input of 7A, and continues incrementing or decrementing the VAR A or VAR B voltage by writing to port 08H or 0AH until the ADC output bit toggles its state.

When the DAC 7541 reference voltage is +10.0V, the DAC 7533 is initially programmed to -10.0V, so Q2 is turned off and the ADC status bit is equal to 1. When the DAC 7541 reference voltages are -9.980V, -5.0V, 0.00V, and +5.0V, DAC 7533 is initialized to +10.0V, so Q2 is turned on, and the ADC is equal to 0.

When VAR A and VAR B are being tested, each DAC 7533 contains five voltage levels, -9.980V, -5.0V, 0.00V, +5.00V, and +10.00V.

TEST STEP INFORMATION:

Step	Reference Voltage	Initial 7533 Data Voltage	Initial ADC Status
1	-9.980V (7541)	0000H (VAR A +10.0V)	0
2	-5.0V (7541)	0000H (VAR A +10.0V)	0
3	-0.000V (7541)	0000H (VAR A +10.0V)	0
4	+5.0V (7541)	0000H (VAR A +10.0V)	0
5	+10.00V (7541)	0FFFH (VAR A -10.0V)	1
6	-9.980V (7541)	0000H (VAR B +10.0V)	0
7	-5.0V (7541)	0000H (VAR B +10.0V)	0
8	-0.000V (7541)	0000H (VAR B +10.0V)	0
9	+5.0V (7541)	0000H (VAR B +10.0V)	0
10	+10.00V (7541)	0FFFH (VAR B -10.0V)	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
DAC 7533 Linearity Test
Voltage Expected     = see.eee
Voltage Lower Limit = suu.uuu
Voltage Upper Limit = sll.lll
Actual Voltage Read = saa.aaa
ADC Status Expected = x
ADC Status Expected = y
```

Where zz should be in the range of 1 through 10

s should be + or -

ee.eee should be in the range of 00.000 through 10.000

uu.uuu should be 10.220, 5.620, 0.500, 4.620, 9.740

ll.lll should be 9.740, 4.620, 0.500, 5.620, 10.240

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1

Threshold Diagnostic Subtest 3

TITLE: THRESHOLD/MUX. LOGIC TEST

TARGET LOGIC: 4D, 5B, 1A, 1D, 1B, 1C, 2A, 2D
5F, 7A, 7E, 5E, 6E, 8B, 8A, 8F
and Q2.

TEST DESCRIPTION:

The Threshold/mux's logic is functionally tested by using the TH0 through TH5 as reference voltages. These voltages are multiplexed through 5F and supplied as the noninverting input to 7A. The DAC 7541 is initially programmed to +10.0V and decrements the output voltages until the ADC output status bit toggles its state.

Reference voltages for -ECL, -TTL, -VAR A, and -VAR B are present for each threshold channel. The -ECL is +1.300V, -TTL is -1.400V, -VAR A is +5.0V, and -VAR B is -5.0V.

Testing occurs for threshold channels TH0 through TH5. The original ADC status bit should be 1 when the DAC 7541 is initialized to +10.0V.

TEST STEP INFORMATION:

Step	Logic	TH Channel	Initialized 7541 Voltage	Initial ADC Status
1	-ECL	0	+10.0V	1
2	-ECL	1	+10.0V	1
3	-ECL	2	+10.0V	1
4	-ECL	3	+10.0V	1
5	-ECL	4	+10.0V	1
6	-ECL	5	+10.0V	1
7	-VAR A	0	+10.0V	1
8	-VAR A	1	+10.0V	1
9	-VAR A	2	+10.0V	1
10	-VAR A	3	+10.0V	1
11	-VAR A	4	+10.0V	1
12	-VAR A	5	+10.0V	1
13	-TTL	0	+10.0V	1
14	-TTL	1	+10.0V	1
15	-TTL	2	+10.0V	1
16	-TTL	3	+10.0V	1
17	-TTL	4	+10.0V	1
18	-TTL	5	+10.0V	1
19	-VAR B	0	+10.0V	1
20	-VAR B	1	+10.0V	1
21	-VAR B	2	+10.0V	1
22	-VAR B	3	+10.0V	1
24	-VAR B	4	+10.0V	1
24	-VAR B	5	+10.0V	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Threshold/Mux. Logic Test
?????? Threshold Testing
TH Channel n Testing
Voltage Expected    = see.eee
Voltage Lower Limit = suu.uuu
Voltage Upper Limit = sll.lll
Actual Voltage Read = saa.aaa
ADC Status Expected = x
ADC Status Expected = y
```

Where zz should be in the range of 1 through 24

?????? should be -ECL, -VAR A, -TTL, -VAR B

n should be in the range of 0 through 5

s should be + or -

ee.eee should be 1.300, 5.000, 1.400, 5.000

uu.uuu should be 0.980, 4.800, 1.720, 5.440

ll.lll should be 1.620, 5.400, 1.080, 4.800

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1

TITLE: SERIAL I/O PORT #1 TEST

TARGET LOGIC: 12D, 14A, 13A, 8E

TEST DESCRIPTION:

Serial I/O port #1 is functionally tested by using USART #1 as a transmitter/receiver to transmit an 8 bit data pattern and receive the transmitted bytes through the wrap back, RS-232 connector within a specified time window (95% through 105%).

The RS-232 wrap back connector is configured as follows:

Pin 2, CTS (clear to send); short to Pin 3, RTS (request to send),

Pin 4, DSR (data set ready); short to Pin5, DTR (data terminal ready),

Pin 6, RxD (received data); short to Pin 20, TxD (transmitted data).

The following patterns are transmitted:

0AAH, 055H, 0CCH, 033H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

The following baud rates are tested:

110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

TEST STEP INFORMATION:

Test Step	Baud Rate	Data Pattern
1 through 12	110	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
13 through 24	150	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
25 through 36	300	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
37 through 48	600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
49 through 60	1200	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
61 through 72	1800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
73 through 84	2400	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
85 through 96	4800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
97 through 108	9600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:

1. If an error for transmitter buffer not empty occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Transmitter Buffer Not Empty
Testing Baud Rate    = bbbb
Status Byte Read     = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

2. If an error for no character received occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
No Character Received
Tesing Baud Rate     = bbbb
Status Byte Read     = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

3. If an error for character received early occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Character Received Early
Tesing Baud Rate         = bbbb
Minimum Expected Count   = eeeee
Actual Software Count    = ccccc
Received Data            = rrH
Transmitted Data         = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 1777, 1296, 641, 320, 156, 118, 79, 40, 20

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

4. If an error for character received late occurs,
the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Character Received Late
Tesing Baud Rate        = bbbb
Maximum Expected Count  = eeeee
Actual Software Count   = ccccc
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 2303, 1701, 859, 417, 204, 155, 99, 53, 28

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

5. If an error for bad character occurs,
the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Bad character Received
Testing Baud Rate       = bbbb
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

TITLE: SERIAL I/O PORT #2 TEST

TARGET LOGIC: 12E, 15B, 13B, 8E, 8D

TEST DESCRIPTION:

Serial I/O port #2 is functionally tested by using USART #2 as a transmitter/ receiver to transmit an 8-bit data pattern and receive the transmitted bytes through the wrap back RS-232 connector within a specified time window (95% through 105%)

The RS-232 wrap back connector is configured as follows:

Pin 2, CTS (clear to send); short to Pin 3, RTS (request to send),

Pin 4, DSR (data set ready); short to Pin 5, DTR (data terminal ready),

Pin 6, RxD (received data); short to Pin 20, TxD (transmitted data).

The following patterns are transmitted:

0AAH, 055H, 0CCH, 033H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

The following baud rates are tested:

110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

TEST STEP INFORMATION:

Test Step	Baud Rate	Data Pattern
1 through 12	110	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
13 through 24	150	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
25 through 36	300	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
37 through 48	600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
49 through 60	1200	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
61 through 72	1800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
73 through 84	2400	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
85 through 96	4800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
97 through 108	9600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:

1. If an error for transmitter buffer not empty occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Transmitter Buffer Not Empty
Testing Baud Rate     = bbbb
Status Byte Read      = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

2. If an error for no character received occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
No Character Received
Tesing Baud Rate      = bbbb
Status Byte Read      = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

3. If an error for character received early occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Character Received Early
Tesing Baud Rate         = bbbb
Minimum Expected Count   = eeeee
Actual Software Count    = ccccc
Received Data            = rrH
Transmitted Data         = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 1777, 1296, 641, 320, 156, 118, 79, 40, 20

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

4. If an error for character received late occurs,
the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Character Received Late
Tesing Baud Rate          = bbbb
Maximum Expected Count    = eeeee
Actual Software Count     = ccccc
Received Data             = rrH
Transmitted Data          = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 2303, 1701, 859, 417, 204, 155, 99, 53, 28

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

5. If an error for bad character occurs,
the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Bad character Received
Testing Baud Rate         = bbbb
Received Data             = rrH
Transmitted Data          = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

Threshold Diagnostic Subtest 6

TITLE: TIMER 8253 COUNTER 0 TEST

TARGET LOGIC: 13F, 8D, 8E and GATE/ logic from control board

TEST DESCRIPTION:

The timer 8253 counter 0 is functionally tested by programming counter 0 to to mode 1 (programmable one shot mode), and triggering GATE0 from control board GATE/ logic. The counter 0 is then verified by reading the latched count after GATE0 been triggered.

The terminal count patterns tested are :

8000H, 4000H, 2000H, 1000H, 0800H, 0400H, 0200H, 0100H,
0080H, 0040H, 0020H, 0010H, 0008H, 0004H, 0002H, 0001H.

There are two methods for testing counter 0 in mode 1:

1. After loading terminal count, trigger GATE0 from low to high.

2. After loading terminal count, trigger GATE0 from low to high two times. The second trigger should cause the counter to reset to the terminal count value.

TEST STEP INFORMATION:

Test Step	Terminal Count Programmed	Rising Edge Trigger Pulses
1	8000H	1
2	4000H	1
3	2000H	1
4	1000H	1
5	0800H	1
6	0400H	1
7	0200H	1
8	0100H	1
9	0080H	1
10	0040H	1
11	0020H	1
12	0010H	1
13	0008H	1
14	0004H	1
15	0002H	1
16	0001H	1
17	8000H	2
18	4000H	2
19	2000H	2
20	1000H	2
21	0800H	2
22	0400H	2

23	0200H	2
24	0100H	2
25	0080H	2
26	0040H	2
27	0020H	2
28	0010H	2
29	0008H	2
30	0004H	2
31	0002H	2
32	0001H	2

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Timer 8253 Counter 0 Test
Programmable One Shot Mode
Testing Terminal count = ccccH
Expected High Count    = eeeeH
Expected Low Count     = llllH
Actually Read Count    = rrrrH
```

where zz should be in the range of 1 through 32

cccc should be 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100,
0080, 0040, 0020, 0010, 0008, 0004, 0002, 0001.

eeee should be 7EC8, 3EC8, 1EC8, 0EC8, 06C8, 02C8, 00C8, FFC8,
FF48, FF08, FEE8, FED8, FED0, FECC, FECA, FEC9.

or 7FDD, 3FDD, 1FDD, 0FDD, 07DD, 03DD, 01DD, 00DD,
005D, 001D, FFFD, FFED, FFE5, FFE1, FFDF, FFDE.

llll should be 7EB8, 3EB8, 1EB8, 0EB8, 06B8, 02B8, 00B8, FFB8,
FF38, FEF8, FED8, FEC8, FEC0, FEBC, FEBA, FEB9.

or 7FCD, 3FCD, 1FCD, 0FCD, 07CD, 03CD, 01CD, 00CD,
004D, 000D, FFED, FFDD, FFD5, FFD1, FFCF, FFCE.

rrrr should be in the range of 0000 through FFFF

TITLE: GPIB INTERNAL CONTROL LINES TEST

TARGET LOGIC: 15F, 17F, 16F, 16D

TEST DESCRIPTION:

The GPIB internal control lines are functionally tested by writing the local control bit true. The control bit is then verified by reading back the control status bit.

There are 5 control lines being tested as follows:

'catn', 'cifc', 'cren', 'srq', 'end'.

NOTE: If the 'cacs' line is not true, the lines for 'catn', 'cifc', 'cren' and 'srq' are also not true.

TEST STEP INFORMATION:

Test Step	Control Bit
1	'catn'
2	'cifc'
3	'cren'
4	'srq'
5	'end'

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Internal Control Lines
Status Port Address 01H
Bit 7 through Bit 3 is :
atn  srq  ifc  ren  eoi
"????" and "cacs" Logic Test
"????" Status Expected = ssssssssB
"????" Status Read     = rrrrrrrrB
Falling Time Constant  = ttttt
"????" Status Expected = eeeeeeeeB
"????" Status Read     = vvvvvvvvB
Rising Time Constant   = ccccc
```

where: zz should be in the range of 1 to 5

???? should be catn, cifc, cren, srq, end.

ssssssss should be 10000000, 00100000, 00010000, 01000000, 00001000.

rrrrrrrr should be 00000000 through 11111111.

ttttt should be in the range of 00000 through 65535.

eeeeeeee should be 00000000.

vvvvvvvv should be 00000000 through 11111111.

ccccc should be in the range of 00000 through 65535.

NOTE: Falling and rising time constants are for diagnostic reference only.

Threshold Diagnostic Subtest 8

TITLE: GPIB INTERNAL MPU INTERRUPT TEST

TARGET LOGIC: 15F, 17F, 16F, 15D, 17D, 21D, 17B,
18B, 19B, 20A, 20B, 21A, 19A, 20A, 16B, 21F

TEST DESCRIPTION:

The GPIB internal MPU interrupt is functionally tested by writing local control bit true and local command bits true. The interrupt status bit is then verified by reading the interrupt status.

There are four MPU interrupt logic conditions being tested: 'tint', 'srint', 'nrint' and 'cint'. (The 'lint' logic condition is associated with the GPIB external handshake function which is not tested.)

The 'INTR1/' test is associated with the 'tint',' srint', 'nrint' and 'cint' interrupt logic conditions.

TEST STEP INFORMATION:

Test Step	MPU Interrupt Logic
1	'tint' and 'INTR1/'
2	'srint' and 'INTR1/'
3	'nrint' and 'INTR1/'
4	'cint' and 'INTR1/'

ERROR MESSAGE:

1. If an INTR1/ error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Internal Interrupt Line
gint/ lint tint cint nrint srint get/ nins/
"?????" Interrupt Line Test
GPIB INTR1/ Not Generated
```

where zz should be in the range of 1 through 4

????? should be tint, srint, nrint, cint.

2. If an interrupt status error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Internal Interrupt Line
gint/ lint tint cint nrint srint get/ nins/
"?????" Interrupt Line Test
Status 1 Expected   = aaaaaaaaB
Status 1 Read       = bbbbbbbbB
Status 2 Expected   = cccccccB
Status 2 Read       = dddddddB
Status 3 Expected   = eeeeeeeeB
Status 3 Read       = ffffffffB
Status 4 Expected   = gggggggB
Status 4 Read       = hhhhhhhhB
```

where zz should be 1 through 4

????? should be tint, srint, nrint, cint

aaaaaaaa should be 10000010.

cccccccc should be 11111111, 10000010.

eeeeeeee should be 00100010, 00000110, 00001010, 00010010.

gggggggg should be 10000010.

bbbbbbbb should be in the range of 00000000 through 11111111

dddddddd should be in the range of 00000000 through 11111111

ffffffff should be in the range of 00000000 through 11111111

hhhhhhhh should be in the range of 00000000 through 11111111

TITLE: GPIB INTERNAL DATA REGISTER TEST

TARGET LOGIC: 18E, 19E, 18D, 19D, 20E, 21E, 20F

TEST DESCRIPTION:

The GPIB internal data register is functionally tested by writing a data byte pattern to the data register or parallel poll response register. The data is then verified by reading the data from the input register.

There are 12 data patterns tb be tested :

0AAH, 55H, 0CCH, 33H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

There are two output registers to be tested :

1. Data output register (18E)

2. parallel poll response register (19E).

TEST STEP INFORMATION:

Test Step	Register Under Test	Data Pattern
1	data output register	0AAH
2	data output register	55H
3	data output register	0CCH
4	data output register	33H
5	data output register	01H
6	data output register	02H
7	data output register	04H
8	data output register	08H
9	data output register	10H
10	data output register	20H
11	data output register	40H
12	data output register	80H
13	parallel poll response	0AAH
14	parallel poll response	55H
15	parallel poll response	0CCH
16	parallel poll response	33H
17	parallel poll response	01H
18	parallel poll response	02H
19	parallel poll response	04H
20	parallel poll response	08H
21	parallel poll response	10H
22	parallel poll response	20H
23	parallel poll response	40H
24	parallel poll response	80H

ERROR MESSAGE:

1. If an error occurs in the data output register, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Data Register Test
Data Out Register Testing
Data Register Expected = eeH
Data Register Read     = rrH
```

where zz should be in the range of 1 through 24

ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

rr should be 00 through FF

2. If an error occurs in the parallel poll response register, the following displayed:

```
* Test FAILED -- Test Step zz
GPIB Data Register Test
Parallel Poll Response
Data Register Expected = eeH
Data Register Read     = rrH
```

where zz should be in the range of 1 through 24

ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

rr should be 00 through FF

K205 STORAGE CONTROLLER BOARD DIAGNOSTIC

DIAGNOSTIC OVERVIEW

This section describes subtests executed on the K205 Storage Controller Board, how error reporting is done, and the concept behind each subtest program.

It should be noted that the K205 Storage Controller Board contains future provisions for installing a UART. This Diagnostic does not test any of the UART components.

There are six subtests written for the Storage Controller Board. Each of these subtests is described individually on the following pages. Parameters for Loop on Error, Error Count, and Pass Count Update are incorporated into each subtest.

All error messages are preceded by a "*". The information messages use the ">" prefix.

Early exit of each subtest is accomplished by pressing the "STOP" key.

ASSUMPTIONS

This series of tests assumes that two other boards are installed in the K205 and are functional, an operational MPU Board as well as the Keyboard/Display Board must be present.

SUBTEST CATEGORIES

1. 6116 Data Integrity Test
2. 6116 Address Integrity Test
3. FDC Seek Test
4. Fixed FDC Write/Read Test
5. Random FDC Write/Read Test
6. FDC/DMA Address Logic Test

ERROR COUNT CATEGORIES

1. Subtest 1
2. Subtest 2
3. Subtest 3
4. Subtest 4
5. Subtest 5
6. Subtest 6
7. Seek Command Error Count
8. Recalibrate Command Error Count
9. Write Command Error Count
10. Read Command Error Count
11. Drive A Error Count
12. Drive B Error Count
13. Side 0 Error Count
14. Side 1 Error Count
15. Soft Error Count
16. Hard Error Count
17. Not Ready Error Count
18. Head Address Error Count
19. Ready Changed State Error Count
20. Missing Address Mark Error Count
21. Write Protected Error Count
22. Sector Not Found Error Count
23. FDC Overrun Error Count
24. FDC Int Timout Error Count
25. Access beyond End of Track Error Count
26. Missing Data Address Mark Error Count
27. Bad Track Error Count
28. Wrong Cylinder Error Count
29. Data Error CRC Error Count
30. Control Mark : Deleted Data Encountered Error Count
31. Unformatted Diskette Error Count
32. Diagnostic Program Error Count

TITLE: 6116 DATA INTEGRITY TEST

PURPOSE:

This subtest confirms the ability of the DMA hardware to sucessfully write data into the 4K area of 6116 RAM. The integrity of the RAM is checked by running several patterns through the Memory.

The RAM is not directly addressable; all access is through the DMA controller.

TARGET HARDWARE: 5D, 5E, 5F, 5H, 6E, 6F, 7E

TEST DESCRIPTION:

It is not possible to Write directly to the 6116 RAMs. All access is through the DMA controller. Data is written to the DMA controller and the controller passes it on to the RAM. Reading is accomplished through the same type of cycle. Various Data patterns are written to the RAM then Read back. If a miscompare occurs, an Error message is printed.

The following is a summary of the Data written to the RAM during each test step:

TEST STEP INFORMATION:

Test Step	Value Written
1	0
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

ERROR MESSAGE:

If any errors are detected, this subtest displays the following message:

```
* Test FAILED--Test Step    xx
RAM Data Error
Value Written  = aaH
Value Read     = bbH
Address Count  = ccccH
DMA Status     = ddH
```

where xx = test step number
aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 0FFF
dd = 00 - FF

TITLE: 6116 ADDRESS INTEGRITY TEST

PURPOSE:

The purpose of this test is to selectivly write 1 byte of Data into the 4K of RAM on the storage controller board which has been preset to zero. Verification is then made to confirm the only place the RAM is written to is the indicated Address.

TARGET HARDWARE: 5D, 5E, 5F, 5H, 6E, 6F, 7E

TEST DESCRIPTION:

It is not possible to Write directly to the 6116 RAMs. All access is through the DMA controller. Data is written to the DMA controller and the controller passes it on to the RAM. Reading is accomplished through the same type of cycle. Various Data patterns are written to the RAM then Read back. If a miscompare occurs, an error message is printed.

All of the RAM in this test is preset to zero then the indicated Address is written with the value 0aah. All of RAM is then Read to verify the written Data. If a miscompare is detected then an error message is displayed.

TEST STEP INFORMATION:

Test Step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H

ERROR MESSAGES:

If any errors are detected, this subtest displays the following message:

```
* Test FAILED--Test Step    xx
All Storage Controller RAM Set to Zero.
Wrote aaH to Address bbbbH
Read  ccH at Address ddddH
```

where xx = test step number
aa = 00 - FF
bbbb = 0000 - 0FFF
cc = 00 - FF
dddd = 0000 - 0FFF

TITLE: FDC SEEK TEST

PURPOSE:

The purpose of this subtest is to verify operation of the seek process on one or both Disk Drives.

TARGET HARDWARE: 2H, 3D, 3E, 3F, 3H, 4C, 4D, 4E, 4F, 7D, 7F

TEST DESCRIPTION:

The FDC is commanded to perform seeks to the given Track as outlined below. Tracks are accessed from Track 0 to 39, and 39 to 0.

Finally, an alternating pattern of seeks spiraling from outermost to innermost Tracks is performed.

As these operations are sent to the FDC controller, the status of the controller is monitored. If an error is detected, an error message is displayed.

This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test Step Number	Drive/Side	Disk Action
1 - 40	A / 0	seek 0-39
41- 80	A / 0	seek 39-0
81- 120	A / 0	spiral inward
121-160	A / 1	seek 0-39
161-200	A / 1	seek 39-0
201-240	A / 1	spiral inward
241-280	B / 0	seek 0-39
281-320	B / 0	seek 39-0
321-360	B / 0	spiral inward
361-400	B / 1	seek 0-39
401-440	B / 1	seek 39-0
441-480	B / 1	spiral inward

ERROR MESSAGES:

If any errors are detected, this subtest will display the error messages found in Appendix 1.

TITLE: FDC WRITE/READ TEST

PURPOSE:

The purpose of this subtest is to verify the Storage Controller Board's capability to Write and Read back information on all Tracks of the Disk Drive.

TARGET HARDWARE: 2H, 3D, 3E, 3F, 3H, 4C, 4D, 4E, 4F, 7D, 7F

2A, 2B, 2C, 3A, 3B

TEST DESCRIPTION:

The FDC is Commanded to Write Data to all Tracks on a given Disk surface on a sector by sector basis. If the Track written to is either Track 0 or Track 39 then all sectors are written to. On other Tracks, only sector 1 is actually tested. The Data is then Read back and compared to the pattern written. If a miscompare occurs, an error message is displayed.

As these operations are sent to the FDC controller, the status of the controller is monitored and if an error is detected an error message is displayed. This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test Step Number	Drive/Side	Disk Action
1 - 40	a/0	Write/Read/compare
41 - 80	a/1	Write/Read/compare
81 - 120	b/0	Write/Read/compare
121 - 160	b/1	Write/Read/compare

ERROR MESSAGES:

If any errors are detected, this subtest will display the following message:

```
* Test FAILED--Test Step    xxx
Sector Compare Error
Track Number          = 0aa
Sector Number         = 00b
Address Within Sector = 0ccch
Wrote ddh
Read  eeh
```

where xxx = test step number
aa = 0 - 39
bb = 0 - 8
ccc = 000 - FFF
dd = 00 - FF
ee = 00 - FF

NOTE: Also see Appendix 1.

TITLE: RANDOM FDC WRITE/READ

PURPOSE:

The purpose of this subtest is to verify the Storage Controller Board's capability to Write and Read back information on 63 random locations of the Disk Drive.

TARGET HARDWARE: 2H, 3D, 3E, 3F, 3H, 4C, 4D, 4E, 4F, 7D, 7F

2A, 2B, 2C, 3A, 3B

TEST DESCRIPTION:

This subtest generates random Data and performs 63 random Read/Write cycles. As Data is written it is then Read back and compared. If a miscompare of data occurs, it is reported via an error message.

As these operations are sent to the FDC controller, the status of the controller is monitored and if an error is detected an error message is displayed.

This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test Step Number	Drive/Side	Disk Action
1- 64	a/0	Write/Read/compare
65- 126	a/1	Write/Read/compare
127- 190	b/0	Write/Read/compare
191- 254	b/1	Write/Read/compare

ERROR MESSAGES:

If any errors are detected, this subtest will display the following message:

```
* Test FAILED--Test Step    xx
Sector Compare Error
Track Number          = 0aa
Sector Number         = 00b
Address Within Sector = cccH
Wrote ddH
Read  eeH
```

where xx = test step number
aa = 0 - 39
bb = 0 - 8
ccc = 000 - FFF
dd = 00 - FF
ee = 00 - FF

NOTE: Also see Appendix 1.

TITLE: FDC/DMA ADDRESS LOGIC

PURPOSE:

The purpose of this subtest is to verify integrity of the Address Counters logic between the DMA controller and the floppy Disk controller.

TARGET HARDWARE: 2H, 3D, 3E, 3F, 3H, 4C, 4D, 4E, 4F, 7D, 7F

2A, 2B, 2C, 3A, 3B

TEST DESCRIPTION:

The Data pattern, 0aah, is written to the indicated Addresses on the Storage Controller Board. The entire RAM contents are written to Track 22 on the first available Drive. The RAM is zeroed out then a Read sector Command is issued. The RAM is then analyzed to determine if the DMA controller has placed Data in the original locations.

As these operations are sent to the FDC controller, the status of the controller is monitored and if an error is detected an error message is displayed.

This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test Step	Address Range
1	0000H - 01FFH
2	0001H - 0200H
3	0002H - 0201H
4	0004H - 0203H
5	0008H - 0207H
6	0010H - 020FH
7	0020H - 021FH
8	0040H - 023FH
9	0080H - 027FH
10	0100H - 02FFH
11	0200H - 03FFH
12	0400H - 05FFH
13	0800H - 09FFH
14	1000H - 11FFH

ERROR MESSAGES:

If any errors are detected this subtest will display the following message:

```
* Test FAILED--Test Step    xx
All storage Controller RAM set to Zero.
Unique Testing Address Range = llllH to hhhhH
Data in Address Range = ddH
Checking Data at Address = aaaaH
Data Expected            = eeH
Data Read                = rrH
```

where
- xx = test step number
- llll = 0000 - 0FFF
- hhhh = 0000 - 0FFF
- dd = AAH
- aaaa = 0000 - 0FFF
- ee = 00 - FF
- rr = 00 - FF

NOTE: Also see Appendix 1.

Error Messages Common to all Disk Activity:

Subtests 3-6 all use a common routine for Disk operations which can generate the following error message:

```
* Test FAILED--Test Step    aa
Retrying Disk Command
Retry Count = b
Disk Command: c
Drive  = d
Head   = e
Track  = 0ff
Sector = g
msg
```

where aa = test step number
b = number of times Disk Command has been attempted
c = seek Command,
Read id Command,
recalibrate Command,
Write Track Command,
Write sector Command,
Read Track Command,
Read sector Command.
d = a or b
e = 0 or 1
ff = 0 to 39
g = 1 to 8

msg = Disk Drive Not Ready.
Head Address Error.
During Command, Ready Changed State.
Missing Address Mark.
Write Protected.
Sector Not Found.
FDC Over-run Error.
Data Error (CRC).
FDC Interrupt Timeout Error.
Access Beyond End of Track.
Missing Data Address Mark.
Bad Track.
Wrong Cylinder.
Data Error (crc).
Control Mark: Deleted Data Encountered.
Not a Formatted Disk.

SCHEMATICS AND DRAWINGS

GENERAL

This chapter contains Schematic Diagrams, Assembly Drawings, Parts Lists and Wire Lists for the K205 Logic Analyzer. The drawings are arranged sequentially by drawing number.

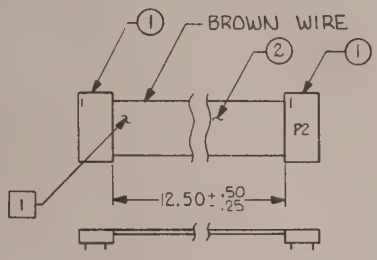
LIST OF DRAWINGS

The following drawings are provided in this chapter:

DRAWING NUMBER	DESCRIPTION
0112-0204-10	Keyboard Cable Assembly
0114-0110-10	Data Board Assembly
0114-0111	Data Board Schematic
0114-0120-10	Control Board Assembly
0114-0121	Control Board Schematic
0114-0160-10/20	Clock Board Assembly
0114-0161	Clock Board Schematic
0114-0170-30	Threshold/GPIB/RS-232 Board Assembly
0114-0171	Threshold/GPIB/RS-232 Board Schematic
0114-0185-80	MPU Board Assembly
0114-0186	MPU Board Schematic
0114-0468-20	DOS Option Assembly
0114-0475-10	DOS Controller Board Assembly
0114-0476	DOS Controller Board Schematic
0114-2010-40	Display Board Assembly
0114-2011	Display Board Schematic
0114-2024-10	Mother Board/Power Supply Cable Assembly
0117-0021-10	Crt Cable Assembly
0117-0040-20	Keyboard Assembly
0117-0099-10	Probe Subassembly
0117-0117-10	Power Switch Cable Assembly
0117-0123-10	CRT Assembly
0117-0133-10	Chassis Ground Cable Assembly
0117-0294-30	Input Cable Set
0117-0294-50	Input Cable Set
0120-0004	Chassis Top Assembly
0120-0025-01	Input Board Assembly
0120-0026	Input Board Schematic
0120-0031-10	Spare Probes, Field Option
0120-0042-01	Input Board Cable Assembly
0120-0043-01	Probe Test Cable Assembly
0120-0044-01	Data Input Cable Assembly
0120-0057-10	K205 Section C Option Assembly
0120-0080-10	Mother Board Assembly
0120-0081	Mother Board Schematic
0120-0145-01	DOS Power Cable Assembly

DWG. NO 0112-0204 | SH 1 | REV F

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
F	3871	REV'D & REDRAWN PER ECO	STM	DGW	6-13-83



1. MARK PART NO. 0112-0204 DASH NO. REV LEVEL AND VENDOR LOGO ON CABLE.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
10	0117-0040	1
10	0112-0120	1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ± 1°; XXX ± .010
HOLE SIZE: 0 .599 ± .001; 600 .999 ± .004; 1.000 1.499 .005

ENG. SERV. | DATE

- 50	- 40	- 30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DRAWN	G.GASSMAN	3-28-77
CHECKED	T. McCANN	3-28-77
PROJ ENG	?	
MANUFACTURING	?	
QUALITY ASSUR		

GOULD biomation

TITLE: KB TO FP CABLE ASSY

SCALE	SIZE	PART NUMBER	REV
	B	0112-0204	F

CODE K100 / K105 | SHEET 1 OF 1

KLINGLER MVBL H

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									2	6000-0114-10	CONN. DIP 16 CONTACT	3M 3416-0000	
2									125"	7100-0095-10	CABLE FLAT 16 COND. 28 AWG	3M 3302/16	

REV	DESCRIPTION	DATE	DWN	CKD
F	REV'D PER ECO 3871	6-13-83	STM	DGW

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
10	0117-0040	1
10	0112-0126	1

DWN	G.GASSMAN	3/28/77
CHK	T. McCANN	3/28/77
ENGR		
MFG.		
Q.A.		

LIST OF MATERIAL

KB TO FP CABLE ASSY

GOULD biomation

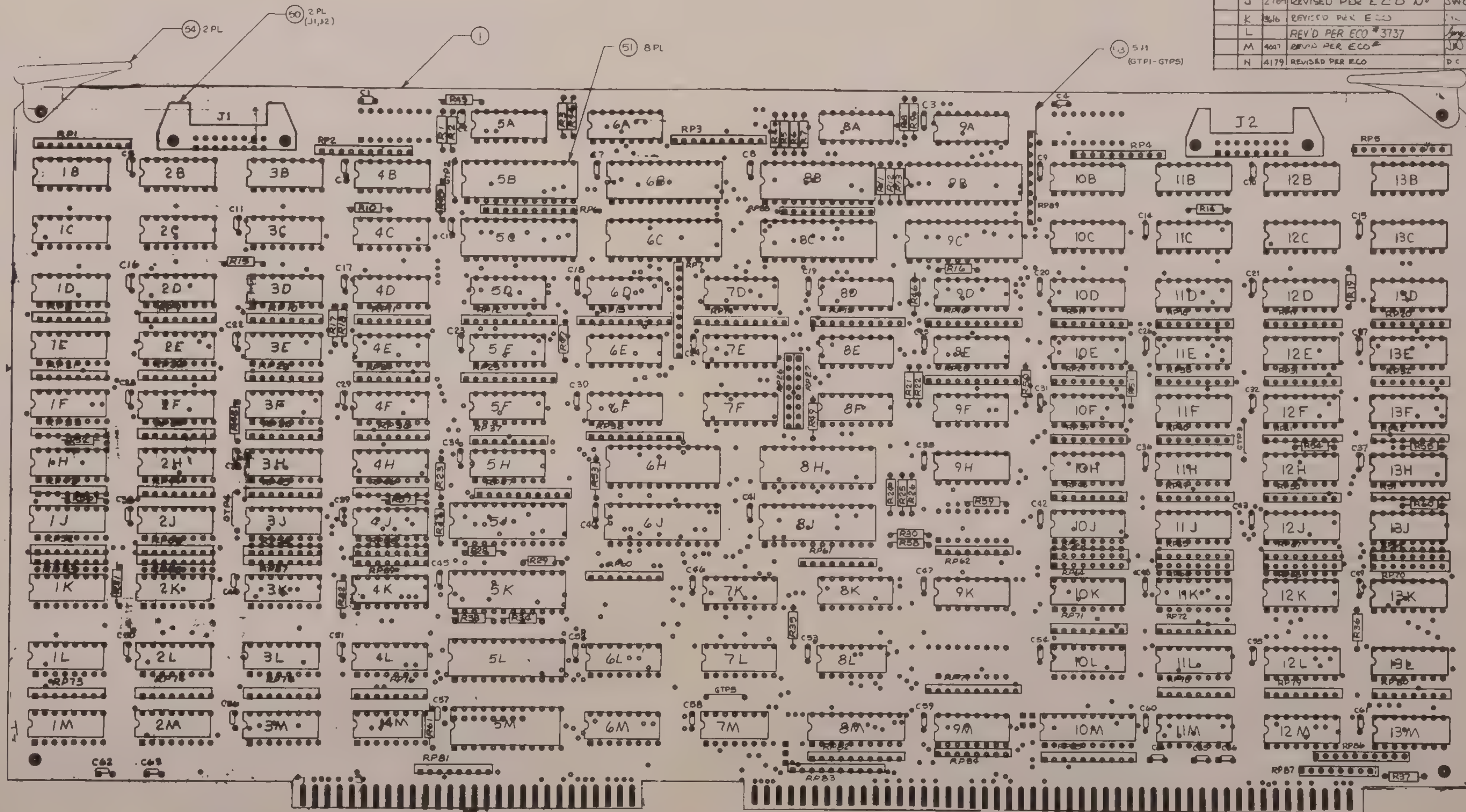
B | 0112-0204 | REV F

MODEL K101/105 | SHEET 1 OF 1

KLINGLER MVBL H10

DWG. NO. 0114-0110 SH 1 REV N

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	H		PROD REL PER FCN #0207	MB	-	2/1/82
	H		REDRAWN	JWC		
	J	2769	REVISED PER ECO N°	JWC	DGW	
	K	3616	REVISED PER ECO		DGW	
	L		REV'D PER ECO #3737			
	M	4047	REV'D PER ECO #		DGW	
	N	4179	REVISED PER ECO	DC		



								1
-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DASH NO	NUMBER	QTY
-10	0114-0002	1
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

ENG SERV — DATE

DRAWN J.W. CARROLL — DATE 5-18-82

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: ASSEMBLY DATA PWB

SCALE	SIZE	PART NUMBER	REV
2:1	D	0114-0110	N

CODE K101-D — SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST
"CER-DIP ONLY" PKGS (FOR 10K ECL DEVICES)			

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0114-0112	PWB				FAB
2												
3												
4						1	1800-0280	I.C.	8L	74S37		
5						2	1800-0240		8M 10M	74LS244		
6						1	1800-0123		7M	74LS14		
7						1	1800-0290	I.C.	9M	74S85		
8												
9												
10						4	1850-0114	I.C.	5A, 6A, 8A, 9A	10016		
11						16	1850-0109		1E-4E, 1F-4F	10106		
12							—		10E-13E, 10F-13F			
13						1	1850-0022		4K	10107		
14						16	1850-0030-10	10121	1C-4C, 1D-4D	10121		
15							—		10C-13C, 10D-13D			
16						5	1850-0104		8K, 9K, 7L, 10L	10124		
17							—		6M			
18						4	1850-0103	I.C.	1M-3M, 11M	10125		

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PRE-PILOT REL PER ERN# 0101	1/17/1			
B	PILOT REL PER ERN# 0130			JL	
C	CHANGE PER ECO 1717	6-2-81			
D	CHANGE PER ECO 1718	6/29			
E	REVISED PER ECO# 1818	9 15 81	MS		
F	REVISED PER ECO# 1842	9 15 81	MS		
G	REVISED PER ECO# 1890	9 15 81	MS		

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
-10	0114-0002	2

		DATE
DRAWN		2-13-81
CHECKED		
ENGINEER		1/7/82
MANUFACTURING		1/7/82
QUALITY ASSURANCE		1/7/82

LIST OF MATERIAL

ASSEMBLY, DATA PWB

biomation

B	0114-0110	REV N

MODEL K101-D | CODE | SHEET 1 OF 4

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
19						8	1850-0102	I.C.	1H-4H, 10H-13H	10130		
20						1	1850-0100	I.C.	7K	10161		
21						6	1850-0105	I.C.	5D.5E, 9E 12M	10173	CERAMIC ONLY	
22							—		13M, 9D			
23						8	1850-0090	I.C.	7L-9L, 10K, 11L 12L, 13L	10174	CERAMIC ONLY	
24						20	1850-0098	I.C.	6E, 7E, 6D, 7D	10176		
25							—		1K-3K, 11K, 12K,	5F, 7F, 8E,	8F	
26							—		5H, 9F, 6F, 9H, 6L,	8D, 13K		
27						8	1850-0097	I.C.	1J-4J, 10J-13J	10231		
28						8	1850-0094	I.C.	1B-4B, 10B-13B	10216		
29						2	6100-0120	SOCKET 16P	4J, 10J			
30												
31						3	1850-0077	I.C.	8H, 5J, 5K	100101		
32						3	1850-0078	I.C.	6J, 8J, 5L	100102		
33						1	1850-0091	I.C.	6H	100155		
34												
35						8	1850-0088	I.C.	5B, 6B, 8B, 9B	10422		
36									5C, 6C, 8C, 9C			

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
H	REVISED PER ECO# 1823	9 15 81	MS		
H	PROD REL PER ERN #0207	1/13/82	MS		
J	REVISED PER E.C.O. NO 2769	3/4/83	JL	DGW	3/4/83
K	REVISED PER E.C.O. # 3616	5/10/83	JL	DGW	5/10/83
L	REV'D PER ECO# 3737	10 28 83	JL	DGW	11/1/83
M	REVID PER ECO# 4047	9/1/84	JL	DGW	9/1/84
N	REVISED PER ECO# 4179	2/27/86	DC	JL	3/4/86

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

		DATE
DRAWN		2-13-81
CHECKED		
ENGINEER		
MANUFACTURING		
QUALITY ASSURANCE		

LIST OF MATERIAL

ASSEMBLY, DATA PWB

biomation

B	0114-0110	REV N

MODEL K101-D | CODE | SHEET 2 OF 4

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
37						4	3700-0039-10	RESISTOR PAK	RP1,2,4,5		56Ω, 10 PIN 9 RES	
38												
39						11	3700-0079	RESISTOR PAK	RP7,12-16,25, 28,38,47,86		75Ω, 10 PIN 9 RES	
40												
41						4	3700-0080	RESISTOR PAK	RP88,89,3,6		100Ω, 10 PIN, 9 RES	
42						8	3700-0044	RESISTOR PAK	RP52,54,56,58, 63,65,67,69		220Ω 8 PIN 4 RES	
43						8	3700-0016	RESISTOR PAK	RP53,55,57,59, 64,66,68,70		1KΩ 8 PIN 7 RES	
44						4	3700-0049	RESISTOR PAK	RP77,82,83,85		3K/62K 10 PIN	
45						1	3700-0057	RESISTOR PAK	RP84		2.2K 8 PIN 7 RES	
46						49	3700-0047	RESISTOR PAK	RP8-11, 17-24, 26, 27, 29-37, 39-46, 48-51, 60-62, 71-76, 78-81, 87		75Ω, 8 PIN, 7 RES	
47							—					
48						58	4010-0103	CAPACITOR	C2,3,5-12,14-61		.01μf 100V	
49						7	4400-0043	CAPACITOR	C1,4,62,63,64,65,66		47μf 6V	
50						2	6000-0374	CONNECTOR	J1, J2	3M	16 PIN HEADER W/EARS	
51						10	6100-0137	SOCKET	X5B, X5C, X6B, X6C,		24 PIN, .4"	
52									X8B, X8C, X9B, X9C, X6J, X6H			
53						5	9000-0054	BUSS WIRE	GTP1-GTP5		GND	
54						2	7000-0120	EJECTOR				

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	DATE
Burt	2-13-81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSEMBLY, DATA PWB

MODEL K101-0

biomation

B | 0114-0110 | REV N

CODE | SHEET 3 OF 4

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55												
56						51	3000-7506	RESISTOR	R1-19, 21-31, 60, 61 33-37, 43-50, 52-56, 58,		75Ω 1/4W 5%	
57												
58												
59						4	3000-5106	RESISTOR	R32, 51, 57, 59		51Ω 1/4W 5%	
60												
61												
62												
63												
64												
65												
66												
67												
68												
69												
70												
71												
72												

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	DATE
	9-15-81
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

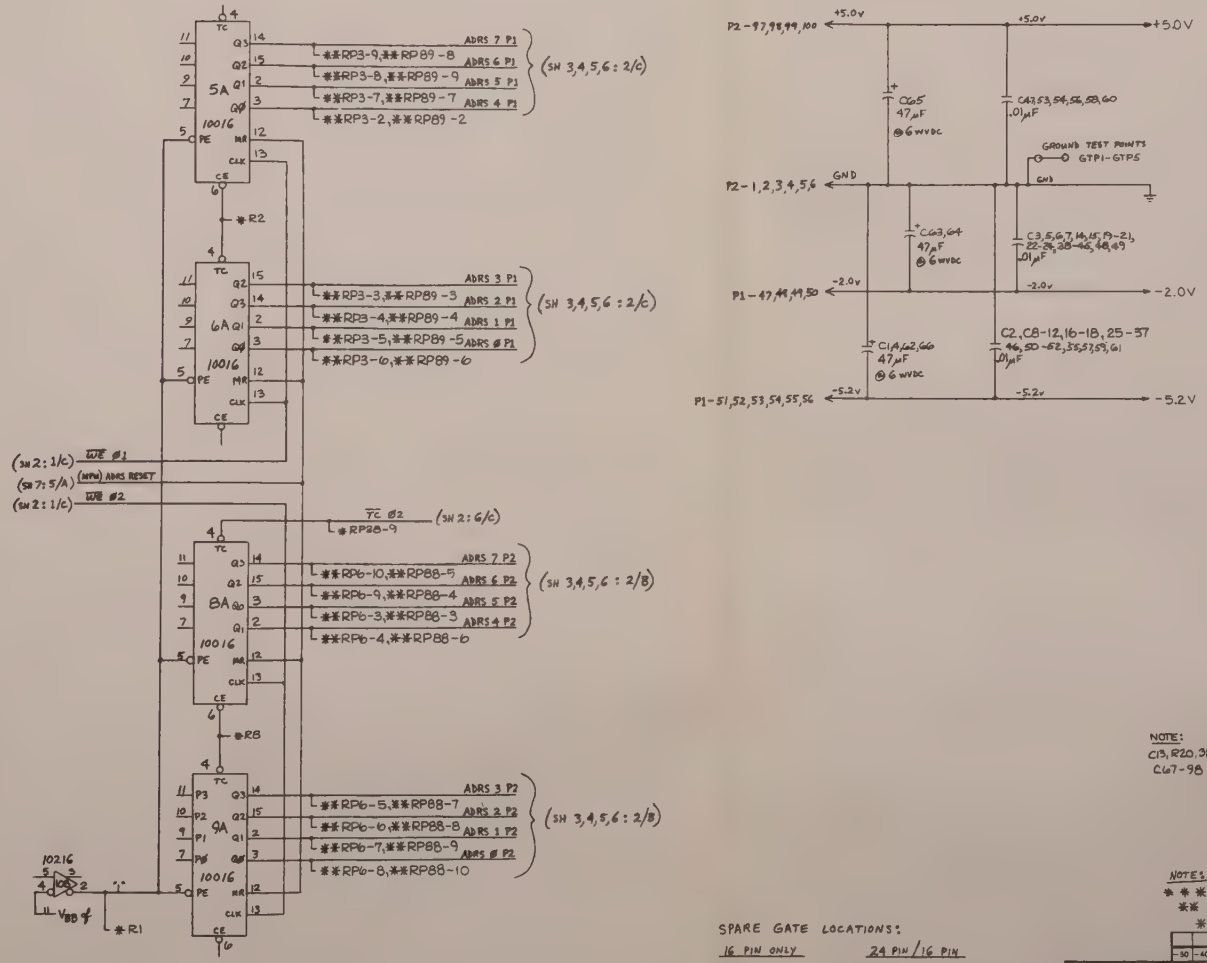
ASSEMBLY DATA PWB

MODEL

biomation

B | 0114-0110 | REV N

CODE | SHEET 4 OF 4



NOTE:
C13, R20, 38, 39, 40, 41, 42 REF DESIG.'s NOT USED.
C67-98 POSITIONS NOT USED.

NOTES: SHEET #8 is WAVE FORMS
* * * = 56Ω RESISTOR PACK @ -2.V
** = 100Ω RES PACK TO -2.0V
* = 75Ω RESISTOR PACK @ -2.V

SPARE GATE LOCATIONS:

16 PIN ONLY	24 PIN / 16 PIN
#1.)	#1.)
#2.)	#2.)
#3.)	#3.)
#4.)	

DWG. NO 0114-0111 SH 1 REV N

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—	PILOT REL ERN #0130	[illegible]		
	B	1717	CHG PER ECO	R.H.		
	C	1718		R.H.		
	D	1818		R.H.		
	E	1842		R.H.		
	F	1890		R.H.		
	G	1823	CHG PER ECO	R.H.		
	G	—	PROD REL PER ERN #0207	[illegible]		[illegible]
	J	2768	REVISED PER ECO No	JWC	DCW	[illegible]
	K	3416	REVISED PER ECO No	JWC	DCW	5-11-83
	L	3737	REVD PER ECO #	[illegible]	DCW [illegible]	[illegible]
	M	4097	REVD PER ECO No	[illegible]	DCW [illegible]	[illegible]
	N	4179	REVISED PER ECO	D.C	[illegible]	[illegible]

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE DIMENSIONS

TOLERANCE
DIMENSIONAL .X ± .1 .XX ± .02 .XXX ± .010 ANGLES ± 1° HOLE SIZE .X .XX ± .005 .XXX ± .004 .XXXX ± .002 ± .001

DASH NO	NUMBER	QTY
-10	0114-0110	—

NEXT ASSEMBLY

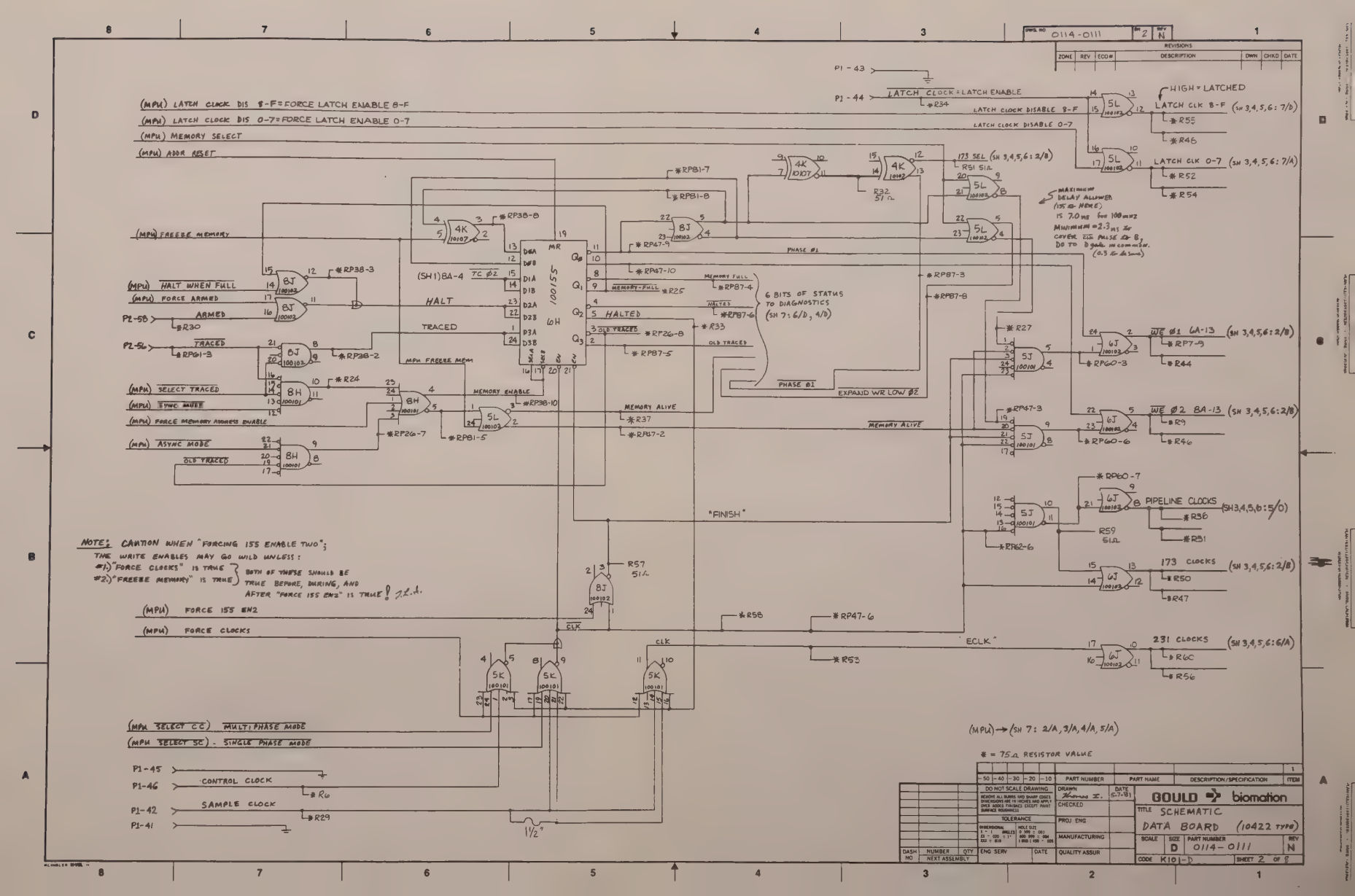
DRAWN [illegible] DATE 5-7-81
CHECKED
PROJ. ENG. [illegible] 1/18/82
MANUFACTURING [illegible] 1/7/82
ENG. SERV. [illegible] DATE 1/7/82
QUALITY ASSUR. [illegible] 1/7/82

GOULD biomation

TITLE SCHEMATIC DATA BOARD (10422 type)

SCALE | SIZE D | PART NUMBER 0114-0111 | REV N

CODE K101-D | SHEET 1 OF 8



DWG NO	SH	REV
0114-0111	2	N

REVISIONS					
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DASH NO	NUMBER NEXT ASSEMBLY	QTY	ENG SERV	DATE	QUALITY ASSUR	

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS AND TOLERANCES ARE APPLY AFTER FINISHES (EXCEPT POINT SURFACE ROUGHNESS)
TOLERANCE
DRAWN Thomas I. DATE 6-7-81
CHECKED
PROJ ENG
MANUFACTURING

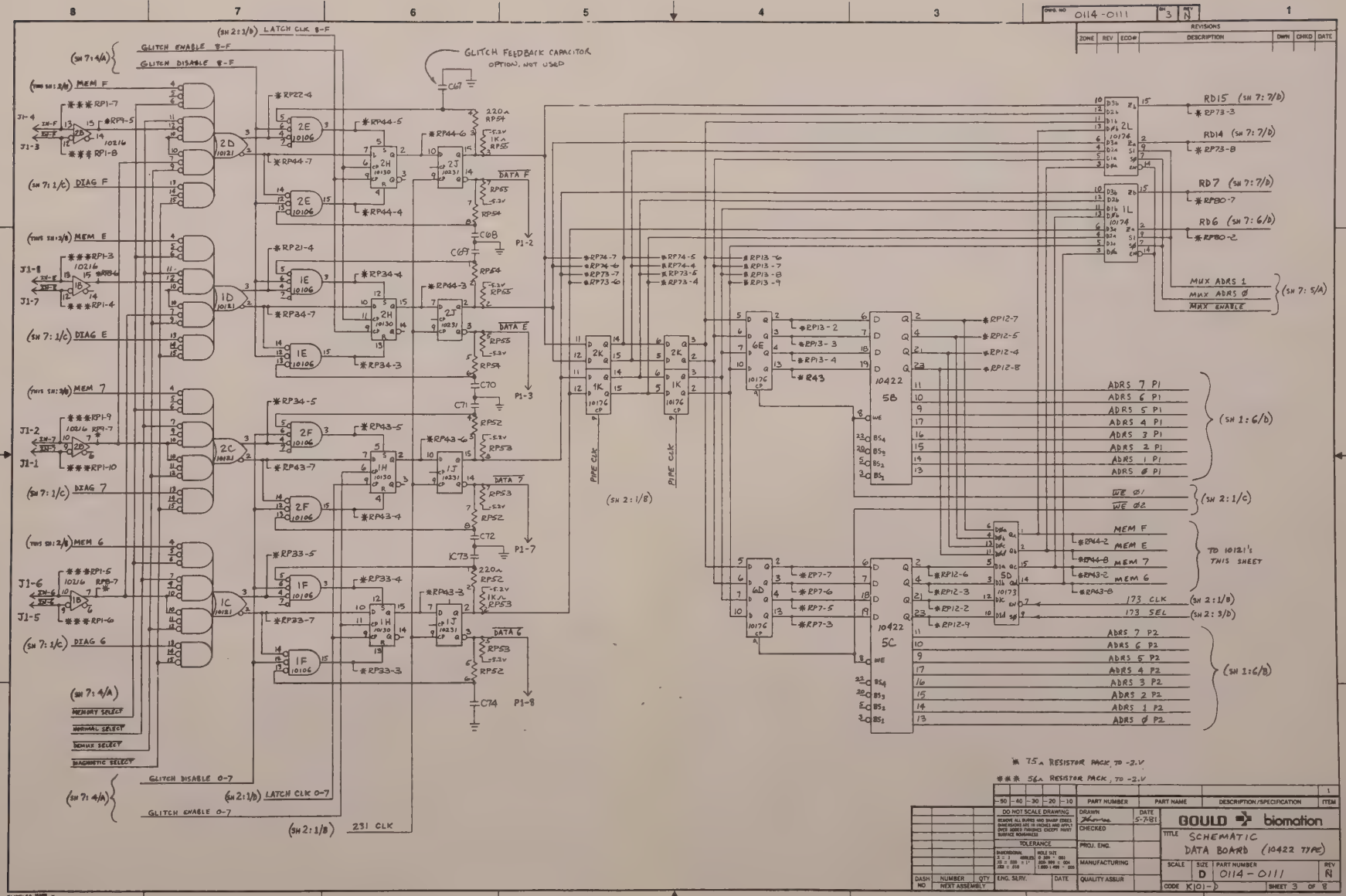
PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

GOULD biomation

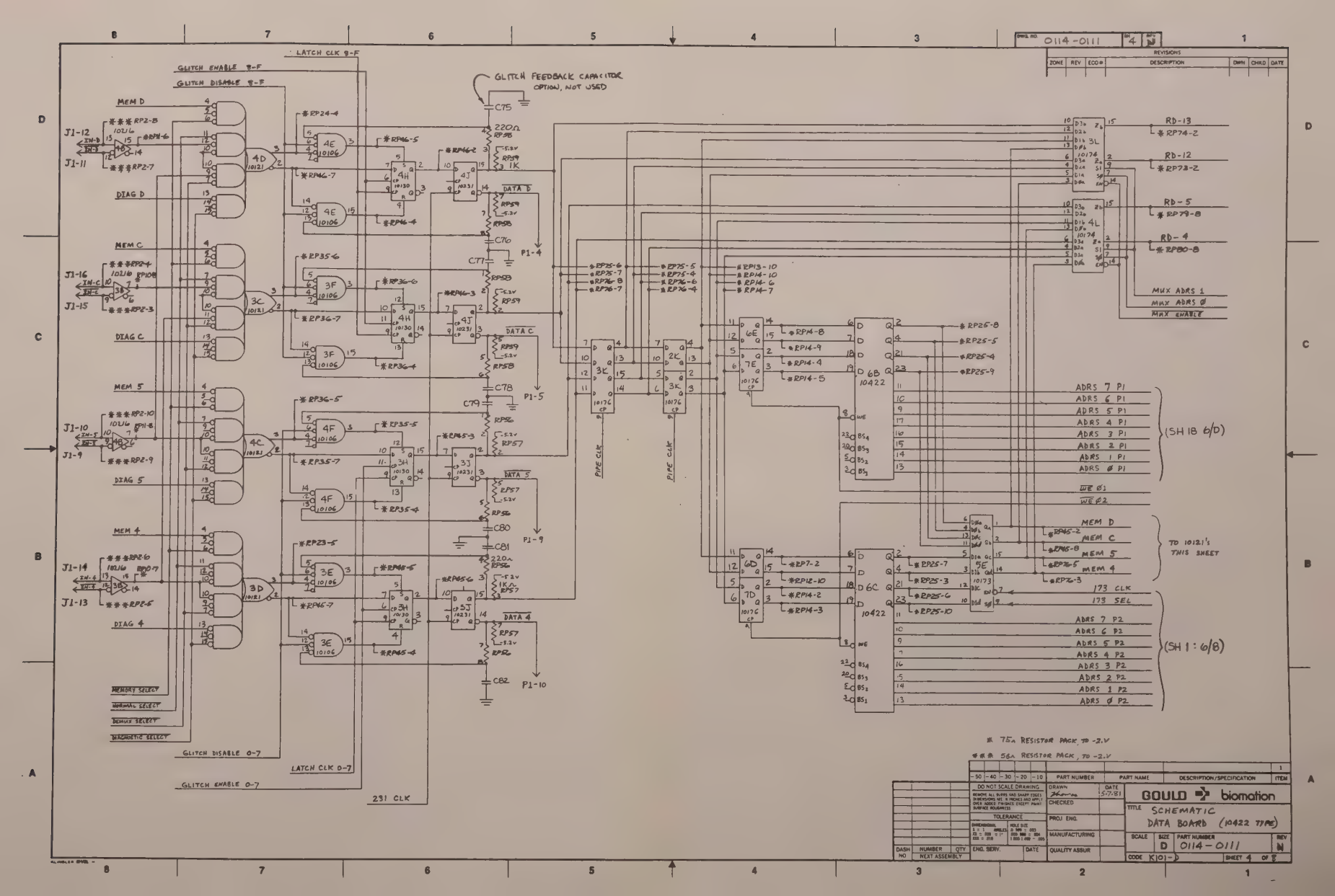
TITLE SCHEMATIC
DATA BOARD (10422 TYPE)

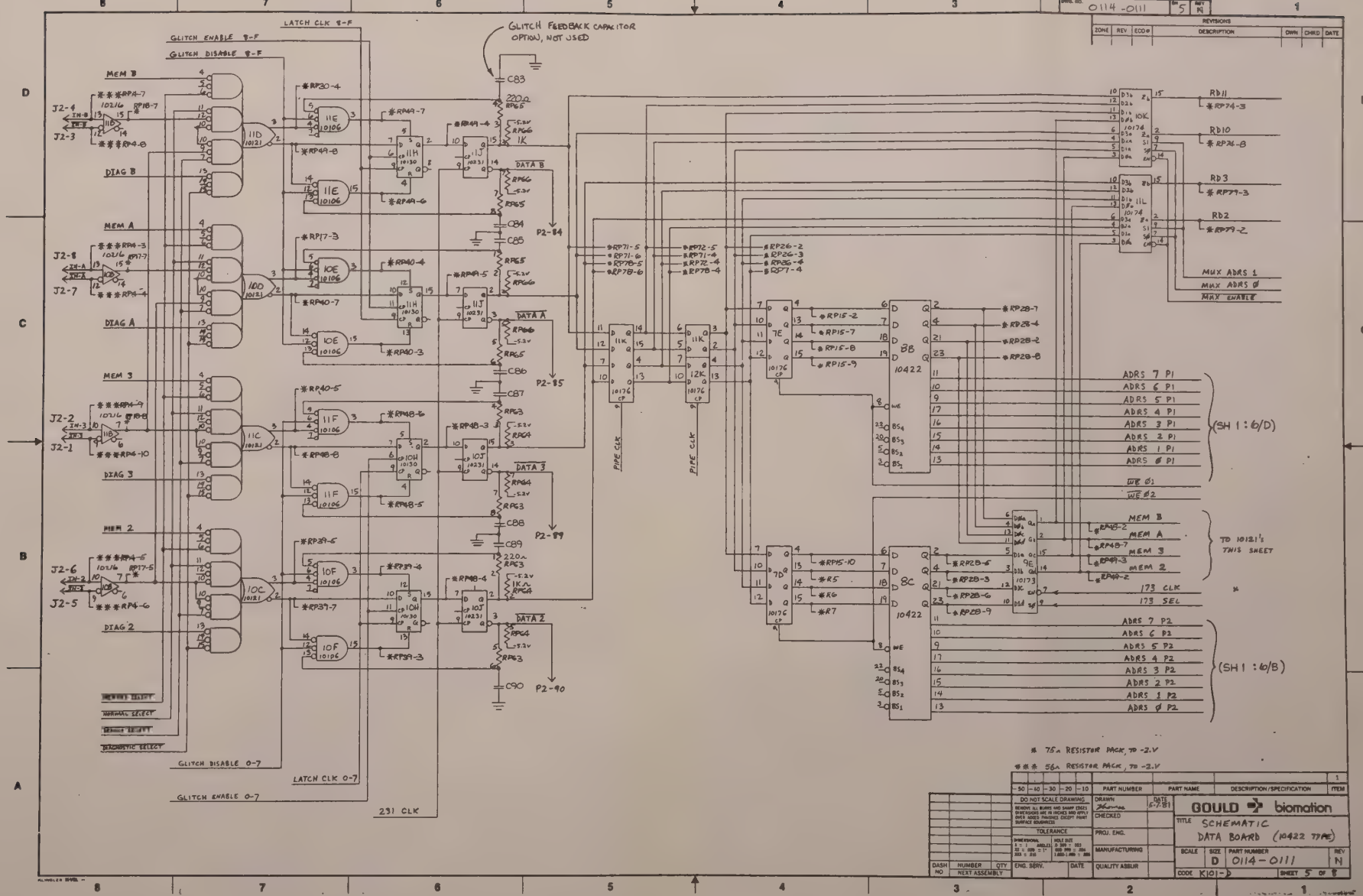
SCALE	SIZE	PART NUMBER	REV
	D	0114-0111	N

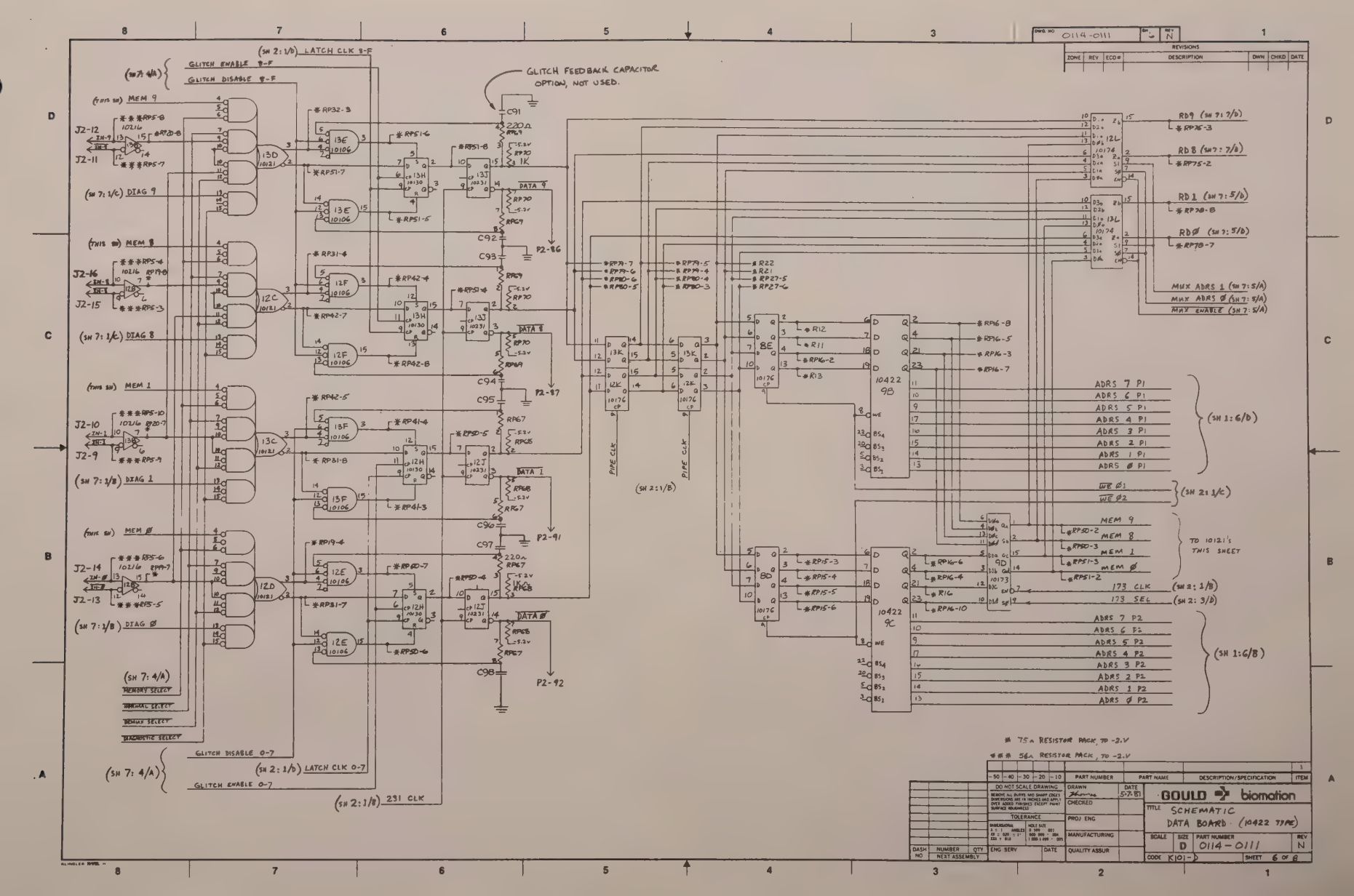
CODE K10-D SHEET 2 OF 8



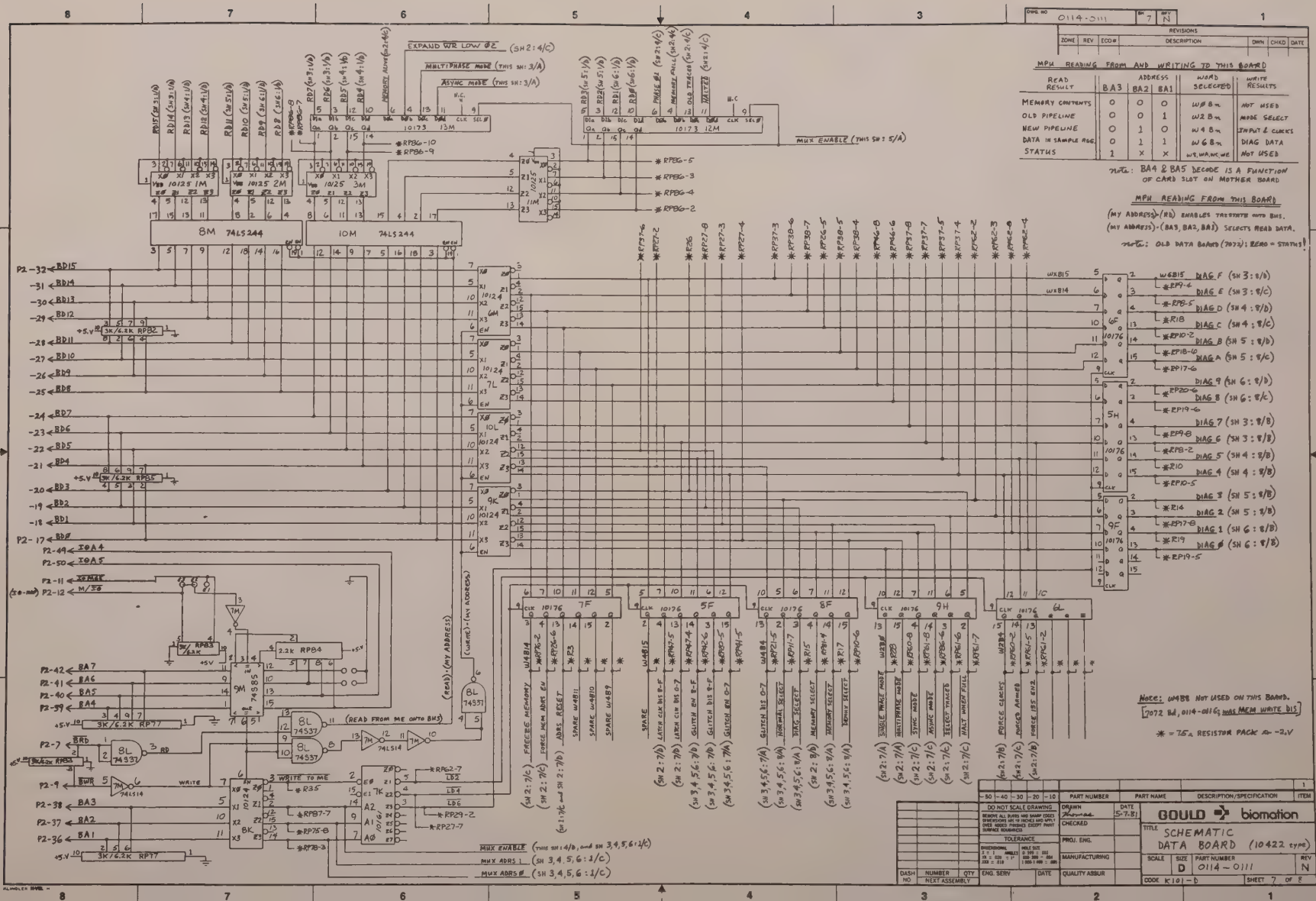
GLITCH FEEDBACK CAPACITOR
OPTION, NOT USED
(SH 2:1/D) LATCH CLK 8-F
GLITCH ENABLE 8-F
GLITCH DISABLE 8-F
(SH 7:4/A)
MEM F
DIAG F
MEM E
DIAG E
MEM 7
DIAG 7
MEM 6
DIAG 6
DATA F
DATA E
DATA 7
DATA 6
P1-2
P1-3
P1-7
P1-8
PIPE CLK
(SH 2:1/B)
RD15 (SH 7:7/D)
RD14 (SH 7:7/D)
RD7 (SH 7:7/D)
RD6 (SH 7:6/D)
MUX ADRS 1
MUX ADRS Ø
MUX ENABLE
(SH 7:5/A)
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
(SH 1:6/D)
WE Ø1
WE Ø2
(SH 2:1/C)
MEM F
MEM E
MEM 7
MEM 6
TO 10121's THIS SHEET
173 CLK
173 SEL
(SH 2:1/B)
(SH 2:3/D)
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
(SH 1:6/B)
(SH 7:4/A)
MEMORY SELECT
NORMAL SELECT
DEMUX SELECT
MAGNETIC SELECT
GLITCH DISABLE 0-7
(SH 2:1/B) LATCH CLK 0-7
GLITCH ENABLE 0-7
(SH 2:1/B) 231 CLK
* 75Ω RESISTOR PACK, TO -2.V
*** 56Ω RESISTOR PACK, TO -2.V
DWG. NO 0114-0111
SH 3
REV N
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DRAWN
DATE 5-7-81
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC
DATA BOARD (10422 TYPE)
SCALE
SIZE D
PART NUMBER 0114-0111
REV N
CODE K101-D
SHEET 3 OF 8


DWG NO. 0114-0111
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
LATCH CLK 8-F
GLITCH ENABLE 8-F
GLITCH DISABLE 8-F
GLITCH FEEDBACK CAPACITOR OPTION, NOT USED
MEM D
MEM C
MEM 5
MEM 4
DIAG D
DIAG C
DIAG 5
DIAG 4
J1-12
J1-11
J1-16
J1-15
J1-10
J1-9
J1-14
J1-13
DATA D
DATA C
DATA 5
DATA 4
P1-4
P1-5
P1-9
P1-10
PIPE CLK
PIPE CLK
MEMORY SELECT
NORMAL SELECT
DEMUX SELECT
DIAGNOSTIC SELECT
GLITCH DISABLE 0-7
LATCH CLK 0-7
GLITCH ENABLE 0-7
231 CLK
RD-13
RD-12
RD-5
RD-4
MUX ADRS 1
MUX ADRS 0
MUX ENABLE
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS 0 P1
(SH 18 6/D)
WE 01
WE 02
MEM D
MEM C
MEM 5
MEM 4
TO 1012.1's THIS SHEET
173 CLK
173 SEL
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS 0 P2
(SH 1 : 6/8)
* 75Ω RESISTOR PACK TO -2.V
*** 56Ω RESISTOR PACK, TO -2.V
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DRAWN CHECKED PROJ ENG. MANUFACTURING QUALITY ASSUR
DATE 5-7-81
GOULD biomation
TITLE SCHEMATIC DATA BOARD (10422 TYPE)
SCALE D SIZE PART NUMBER 0114-0111 REV N
CODE K101-D SHEET 4 OF 8


GLITCH FEEDBACK CAPACITOR OPTION, NOT USED
LATCH CLK 8-F
GLITCH ENABLE 8-F
GLITCH DISABLE 8-F
MEM B
MEM A
MEM 3
MEM 2
DIAG B
DIAG A
DIAG 3
DIAG 2
DATA B
DATA A
DATA 3
DATA 2
P2-84
P2-85
P2-89
P2-90
PIPE CLK
231 CLK
GLITCH DISABLE 0-7
LATCH CLK 0-7
GLITCH ENABLE 0-7
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
WE Ø1
WE Ø2
(SH 1 : 6/D)
TO 10121's THIS SHEET
173 CLK
173 SEL
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
(SH 1 : 6/B)
MUX ADRS 1
MUX ADRS Ø
MUX ENABLE
RD11
RD10
RD3
RD2
* 75Ω RESISTOR PACK, TO -2.V
*** 56Ω RESISTOR PACK, TO -2.V
GOULD biomation
SCHEMATIC
DATA BOARD (10422 TYPE)
0114-0111
SHEET 5 OF 8



DWG NO 0114-0111
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
GLITCH FEEDBACK CAPACITOR OPTION, NOT USED.
(SH 2:1/D) LATCH CLK 8-F
GLITCH ENABLE 8-F
GLITCH DISABLE 8-F
(SH 7:4/A)
(THIS SH) MEM 9
(SH 7:1/C) DIAG 9
(THIS SH) MEM 8
(SH 7:1/C) DIAG 8
(THIS SH) MEM 1
(SH 7:1/B) DIAG 1
(THIS SH) MEM Ø
(SH 7:1/B) DIAG Ø
(SH 7:4/A)
MEMORY SELECT
NORMAL SELECT
DEMUX SELECT
DIAGNOSTIC SELECT
GLITCH DISABLE 0-7
(SH 2:1/D) LATCH CLK 0-7
GLITCH ENABLE 0-7
(SH 2:1/B) 231 CLK
DATA 9
DATA 8
DATA 1
DATA Ø
P2-86
P2-87
P2-91
P2-92
PIPE CLK
(SH 2:1/B)
RD9 (SH 7:7/D)
RD8 (SH 7:7/D)
RD1 (SH 7:5/D)
RDØ (SH 7:5/D)
MUX ADRS 1 (SH 7:5/A)
MUX ADRS Ø (SH 7:5/A)
MUX ENABLE (SH 7:5/A)
ADRS 7 P1
ADRS 6 P1
ADRS 5 P1
ADRS 4 P1
ADRS 3 P1
ADRS 2 P1
ADRS 1 P1
ADRS Ø P1
(SH 1:6/D)
WE Ø1
WE Ø2
(SH 2:1/C)
MEM 9
MEM 8
MEM 1
MEM Ø
TO 10121's THIS SHEET
173 CLK (SH 2:1/B)
173 SEL (SH 2:3/D)
ADRS 7 P2
ADRS 6 P2
ADRS 5 P2
ADRS 4 P2
ADRS 3 P2
ADRS 2 P2
ADRS 1 P2
ADRS Ø P2
(SH 1:6/B)
* 75Ω RESISTOR PACK, TO -2.V
*** 56Ω RESISTOR PACK, TO -2.V
DO NOT SCALE DRAWING
DRAWN
DATE 5-7-81
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
TOLERANCE
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC DATA BOARD (10422 TYPE)
SCALE
SIZE D
PART NUMBER 0114-0111
REV N
CODE K101-D
SHEET 6 OF 8

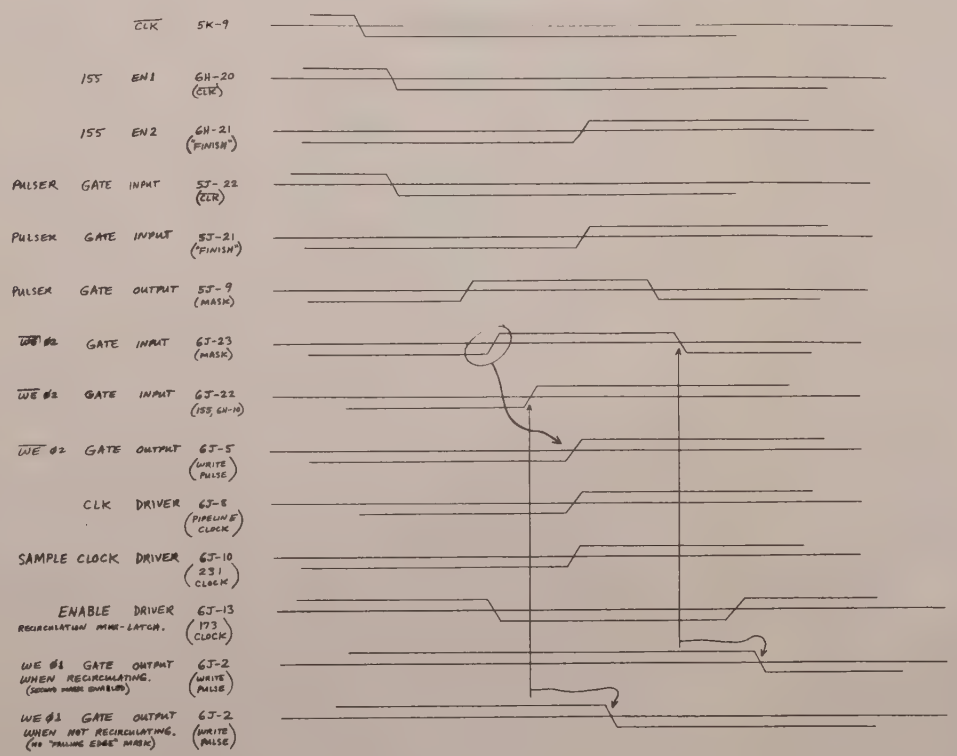

DWG NO 0114-0111
REVISIONS
MPH READING FROM AND WRITING TO THIS BOARD
Note: BA4 & BA5 DECODE IS A FUNCTION OF CARD SLOT ON MOTHER BOARD
MPH READING FROM THIS BOARD
(MY ADDRESS)/RD ENABLES TRISTATE onto BUS.
(MY ADDRESS)-(BA3, BA2, BA1) SELECTS READ DATA.
Note: OLD DATA BOARD (7072): ZERO = STATUS!
EXPAND WR LOW @2
MULTIPHASE MODE (THIS SH: 3/A)
ASYNC MODE (THIS SH: 3/A)
MUX ENABLE (THIS SH: 5/A)
8M 74LS244
10M 74LS244
(READ)-(MY ADDRESS)
(WRITE)-(MY ADDRESS)
(READ FROM ME onto BUS)
2 WRITE TO ME
MUX ENABLE (THIS SH: 4/D, and SH 3,4,5,6: 1/C)
MUX ADRS 1 (SH 3,4,5,6: 1/C)
MUX ADRS 0 (SH 3,4,5,6: 1/C)
Note: U48B NOT USED ON THIS BOARD.
7072 Bd, 0114-0116, HAS MEM WRITE DIS
* = 75Ω RESISTOR PACK to -2V
SCHEMATIC
DATA BOARD (10422 type)
GOULD biomation
SCALE D
SIZE
PART NUMBER 0114-0111
REV N
CODE K101-D
SHEET 7 OF 8

DWG. NO. 0114-0111 | SH 8 | REV N

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DATA BOARD WAVEFORMS



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0 .500 ± .003; .500 .000 ± .004; 1.000 1.400 ± .005

DRAWN: [signature] DATE: 5-7-81

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

ENG SERV | DATE

DASH NO | NUMBER | QTY

NEXT ASSEMBLY

GOULD biomation

TITLE: SCHEMATIC DATA BOARD

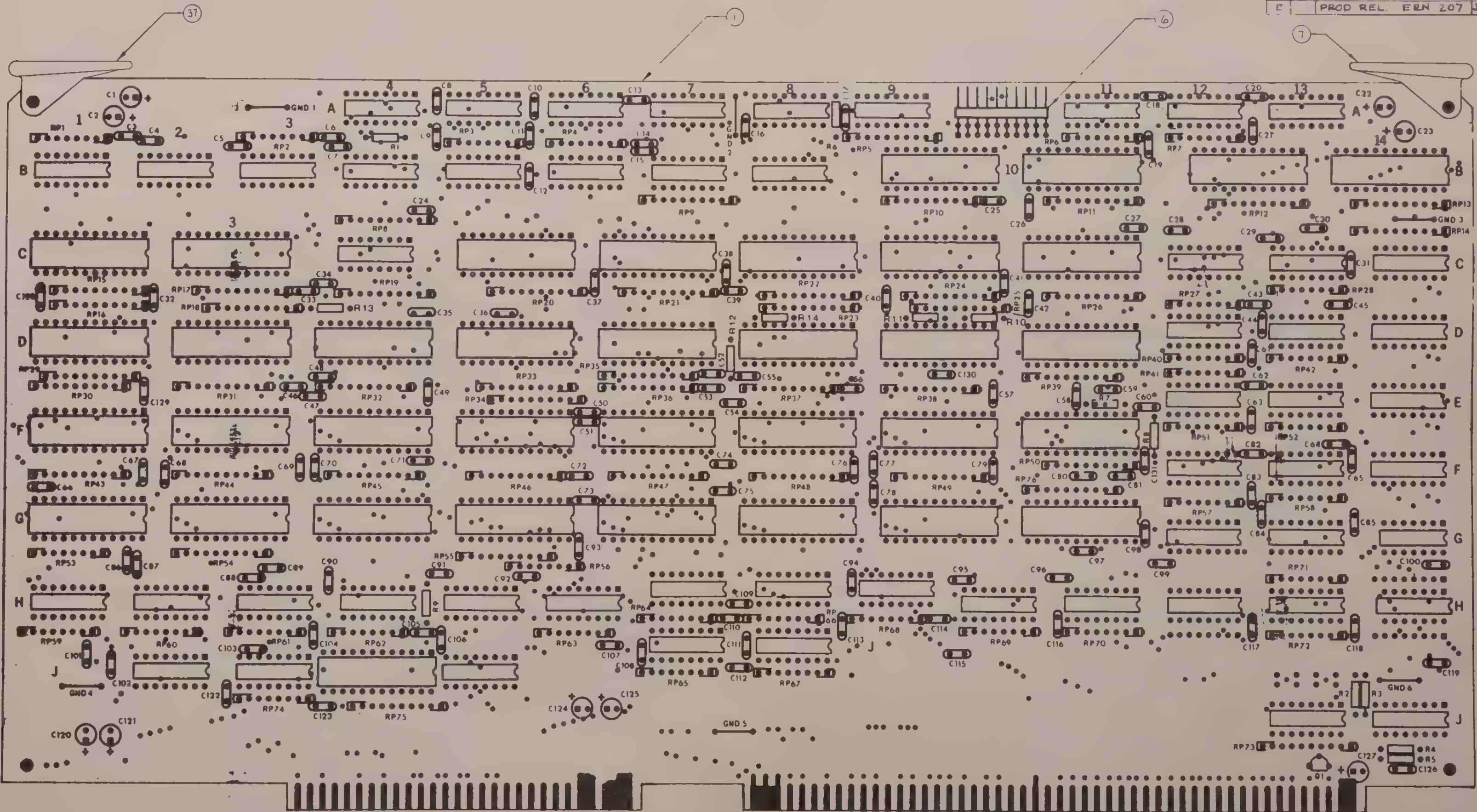
SCALE | SIZE: D | PART NUMBER: 0114-0111 | REV: N

CODE K101-D | SHEET 8 OF 8

F	3/4/?	REVISED PER ECO			
G	3/6/?	REVISED PER ECO			
H	4123	REVISED PER E.C.O Nº	JWC	12/1/83	
J	4288	REVISED PER ECO#			

DWG NO 0114-0120 SH 1 REV J

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	B		PILOT RELEASE ERN Nº 0130	DB		
	C	1725	REVISED PER ECO	SR	DC	5 1 81
	D	1726	REVISED PER ECO	SR	DC	5 1 81
	D	—	REDRAWN	SR	DC	5 1 81
	E	1891	REVISED PER ECO	MB	RD	6 13 81
	F		PROD REL. ERN 207		RG	



NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO	NEXT ASSEMBLY NUMBER	QTY
-20	0114-1002	1
-10	0114-0002	1

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°

HOLE SIZE: 0 .599 .003; .600 .999 .004; 1.000 1.499 .005

ENG SERV — DATE 1/7/82

DRAWN S. RIDDELL — DATE 5 1 81

CHECKED

PROJ ENG — 1/7/82

MANUFACTURING — 1/7/82

QUALITY ASSUR. — 1/7/82

GOULD biomation

TITLE: ASSEMBLY, CONTROL BOARD

SCALE 2:1 | SIZE D | PART NUMBER 0114-0120 | REV J

CODE K101-D | SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1					1	1	0114-0122	PWB				FAB
2					1	1	3700-0057	RES PAK	RP7I		2.2K 8PIN SIP	
3					1	1	1800-0105	IC	14G	74LS00		
4					1	1	1800-0254	IC	13H	74LS85		
5					1	1	1800-0349	IC	12H	7436BA		
6					1	1	6000-0307	HEADER, BARE			20 PIN RT ANGLE	
7					1	1	7000-0120	CARD EJECTOR				
8					2	2	1850-0103	IC	12G, 14J	10125		
9					1	1	-0097		5A	10231		
10					5	5	-0104		3J, 7J, 8J, 10H, 11H	10124		
11					6	6	-0099		4C, 12C, 12D, 12E, 12F, 13J	10164		
12					1	1	-0106		4A	10117		
13					1	1	-0111		11A	10103		
14					4	4	-0114		13C, 13D, 13E, 13F	10016		
15					12	12	-0098		1H, 2H, 2J, 3H, 4H, 6H 7H, 8H, 9H, 6A, 7A, 12A	10176		
16					9	9	-0077		1D, 3D 4D, 5F, 7D 8D, 9B, 9D, 11D	100101		
17					11	11	-0078		1C, 3C, 4J, 5C, 5D, 7C, 8C, 9C, 11B, 11C, 11F	100102		
18					1	1	1850-0079	IC	11G	100112		

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PRE PILOT REL ERN # 0101	2 11 81	MS		
B	PILOT REL ERN # 0130	4-8-81	MS	JL	
C	REVISED PER ECO N° 1725	6 CHG	MS	BD	
D	REVISED PER ECO N° 1726	6-8-81	MS	BD	
E	REVISED PER ECO N° 1891	8-19-81	MS	BD	
E	PROD REL PER ERN #0207	12/31/82	MS	BD	
F	REVISED PER ECO # 2453	12/13/82	J.G.	BD	12/14/82

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-20	0114-1002	1
-10	0114-0002	1

	DRAWN	DATE
	J.W. CARROLL	4-9-81
	CHECKED	12/4/82
	ENGINEER	1-7-83
	MANUFACTURING	1/7/83
	QUALITY ASSURANCE	1/7/83

LIST OF MATERIAL
ASSEMBLY - CONTROL BOARD

biomation

B | 0114-0120 | REV J

MODEL K101-D | CODE | SHEET 1 OF 3

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19					—	12	1850-0088	IC	1F, 1G, 3F, 3G, 4F, 4G, 7F, 7G, 8F, 8G, 9F, 9G	10422		
20					10	10	1850-0089-10	IC	1B-8B, 8A, 9A		F10145ADC	
21					7	7	1850-0089-20	IC	5H, 5J, 13A, 14C-14F		HD10145	
22					3	3	1850-0091		12B, 14B, 5G	100155		
23					1	1	1850-0100	IC	13G	10161		
24					122	122	4010-0103	CAP	C3-21, 24-119, 122, 123, 126, 128-131		.01uf, 100V	
25					9	9	4400-0043	CAP	C1, 2, 22, 23, 120, 121, 124, 125, 127		47uf, 6V	
26					1	1	1400-0019	TRANSISTOR	Q1	2N3906		
27					8	-	1850-0088	IC	4F, 4G, 7F, 7G, 8F 8G, 9F, 9G	10422		
28					6	6	3700-0088	RES PAK	RP 65, 67, 69, 70, 72, 74		3K/6.2K, 8 PIN SIP	
29					25	25	3700-0091	RES PAK	RP1-4, 6, 7, 27, 28, 40-42 51-53, 56-64, 66, 68		68 Ω, 8 PIN SIP	
30					44	44	3700-0092	RES PAK	RP5, 8-26, 29-39, 76 43-50, 54, 55, 73, 75		68Ω, 10 PIN SIP	
31					1	1	3000-2001	RESISTOR	R1		2K, 1/4W 5%	
32					1	1	-2006		R2		20Ω	
33					1	1	-1800		R3		180Ω	
34					1	1	-3300		R4		330Ω	
35					1	1	3000-5106	RESISTOR	R5		51Ω, 1/4W 5%	
36					12	12	6100-0137	SOCKET	ALL 10422		24 PIN (.4")	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	REVISED PER ECO # 03512	12-15-82	J.G.		12/14/82
H	REVISED PER ECO N° 4123	10-2-83	MS	BD	10-11-83
J	REVISED PER ECO # 4288	1-27-84	JG	BD	4/15/84

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL
ASSEMBLY - CONTROL BOARD

biomation

B | 0114-0120 | REV J

MODEL K101-D | CODE | SHEET 2 OF 3

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37					1	1	0112-0228-01	EJECTOR, STAMPED			"A1"	
38					17	17	6100-0120	SOCKET	ALL 10145		16 PIN	
39					6	6	9000-0054	GND WIRE	GND 1-6			
40												
41					1	1	6100-0119	SOCKET	X14H		14 PIN	
42					1	1	3000-1002	RESISTOR	R14		10K, 1/4W, 5%	
43					1	1	1800-0280	IC	14H		7437	
44												
45					6	6	3000-6806	RESISTOR	R6,9 T013		68Ω, 1/4W, 5%	
46					2	2	3000-6800	RESISTOR	R7,8		680Ω, 1/4W, 5%	
47												
48												
49												
50												
51												
52												
53												
54												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

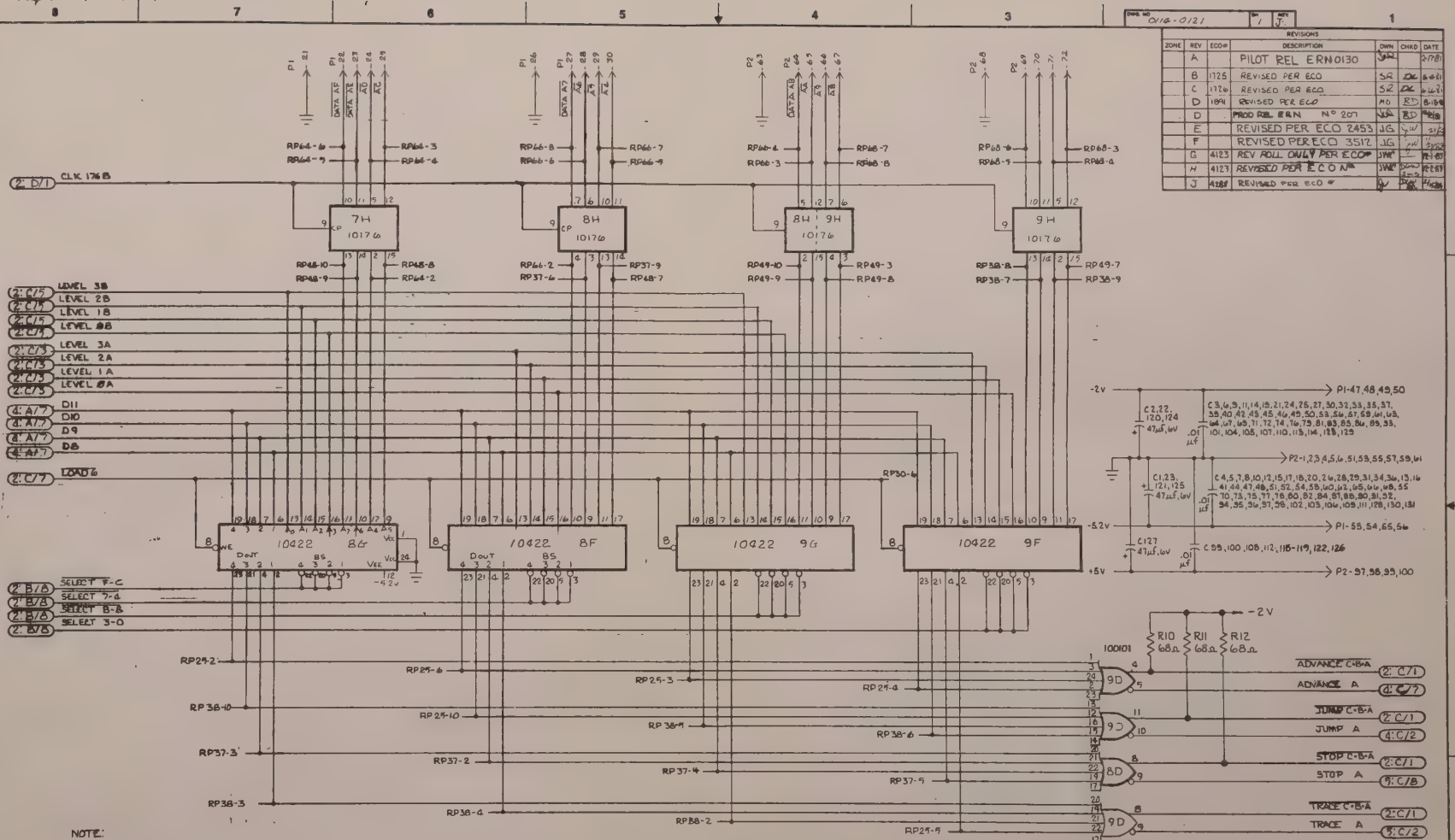
	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	
.	

LIST OF MATERIAL
ASSEMBLY, CONTROL BOARD

biomation

B	0114-0120	REV J

MODEL K101-D | CODE | SHEET 3 OF 3



NOTE:

1. ALL RESISTOR PAKS TIED TO (-2V) EXCEPT FOR RP 59,69,70,72,73,75,76,77 TIED TO (+5V).
2. MAY USE HD10145 IC's IN PLACE OF 10145A IC's; ONLY IN LOCATIONS 5H, 5J, 13A, 14C-14F.
3. R6 IS USED AS A TEST POINT AT TOP OF BOARD, SHT 6.
4. RP34-4 AND RP34-2 WERE CONNECTED ON ETCH B.
5. RP17-7 WAS CONNECTED ON ETCH B.

DWG NO 0114-0121 SH 1 REV J

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT REL ERN0130	JW		2-17-81
	B	1725	REVISED PER ECO	SR	DK	6-6-81
	C	1726	REVISED PER ECO	SR	DK	6-6-81
	D	1891	REVISED PER ECO	MO	RD	8-18-81
	D		PROD REL ERN Nº 207	JW	RD	[illegible]
	E		REVISED PER ECO 2453	JG	JW	[illegible]
	F		REVISED PER ECO 3512	JG	JW	[illegible]
	G	4123	REV ROLL ONLY PER ECO#	JWC		12-1-83
	H	4123	REVISED PER ECO Nº	JWC	[illegible]	12-2-83
	J	4281	REVISED PER ECO #	JW	[illegible]	[illegible]

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES ± .25 ± .005 ± 1° .XX ± .010 .XXX ± .010 | HOLE SIZE ± .005 ± .003 .005 .001 ± .005 .001 ± .005 ± .005

DRAWN [signature] DATE 4-11-81
CHECKED [signature] 4-16-81
PROJ ENG [signature] 1/18/82
MANUFACTURING [signature] 1/17/82
QUALITY ASSUR [signature] 1/7/82

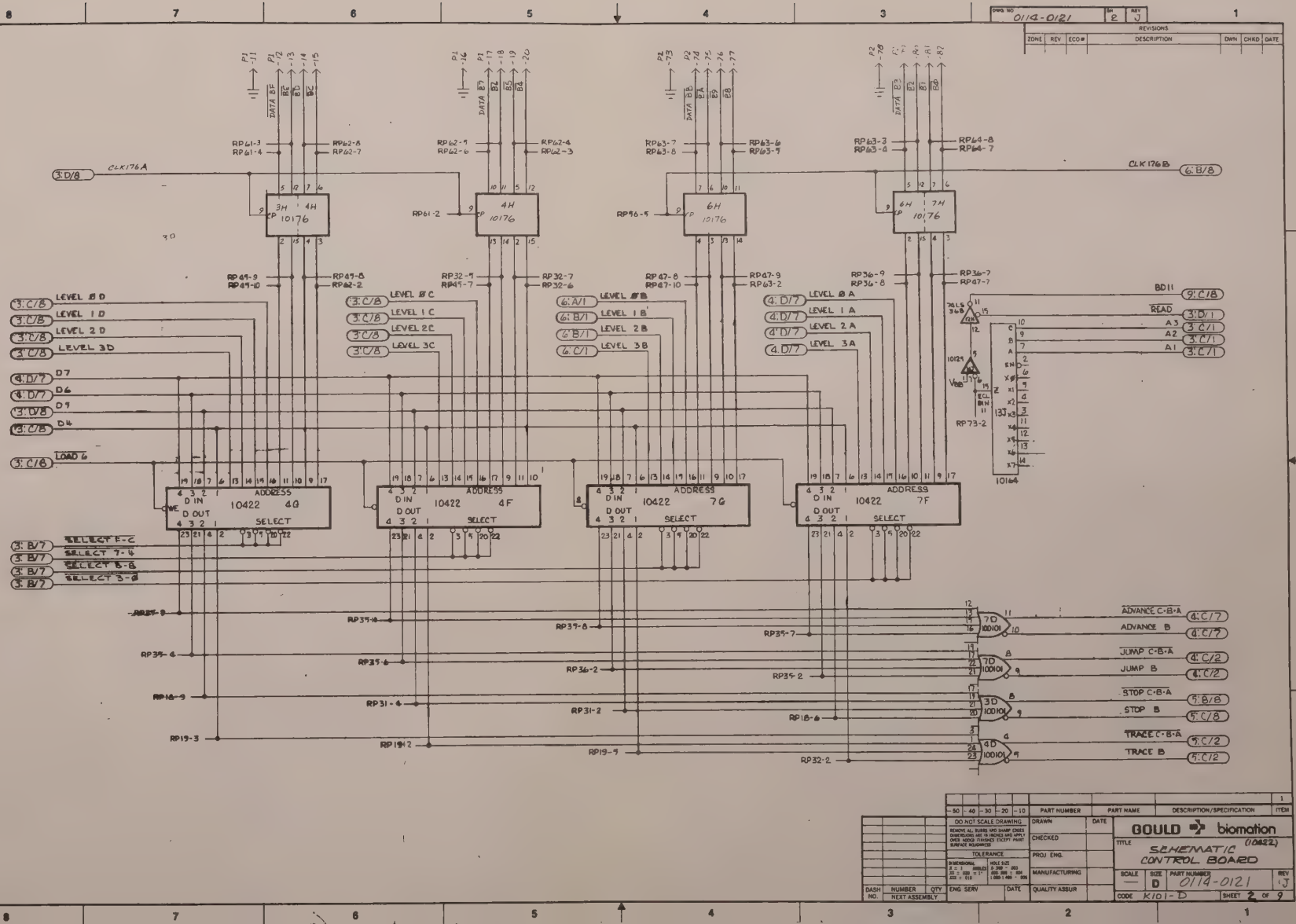
GOULD biomation

TITLE SCHEMATIC CONTROL BOARD

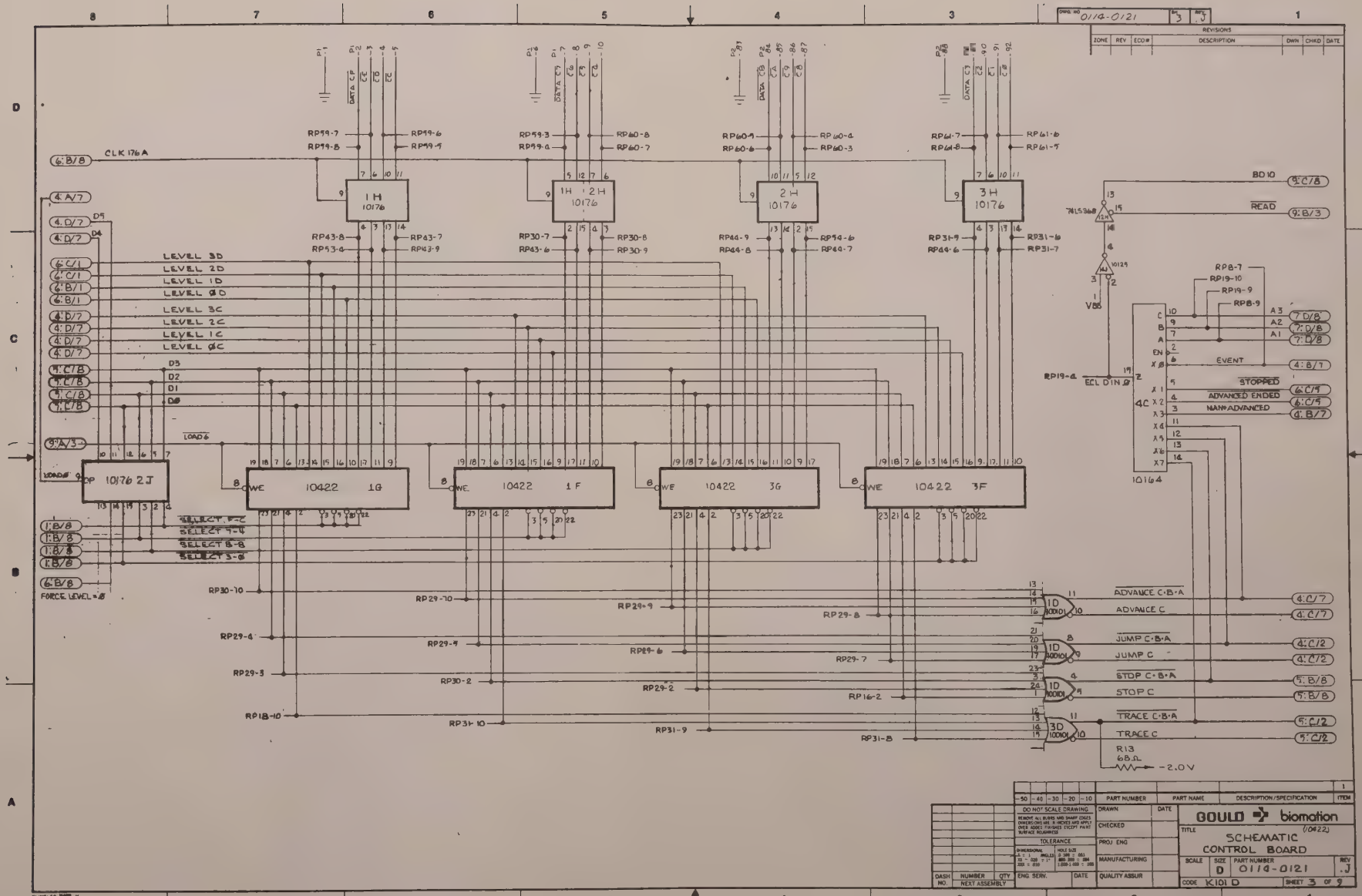
SCALE ~ SIZE D PART NUMBER 0114-0121 REV J

CODE K101-D SHEET 1 OF 9

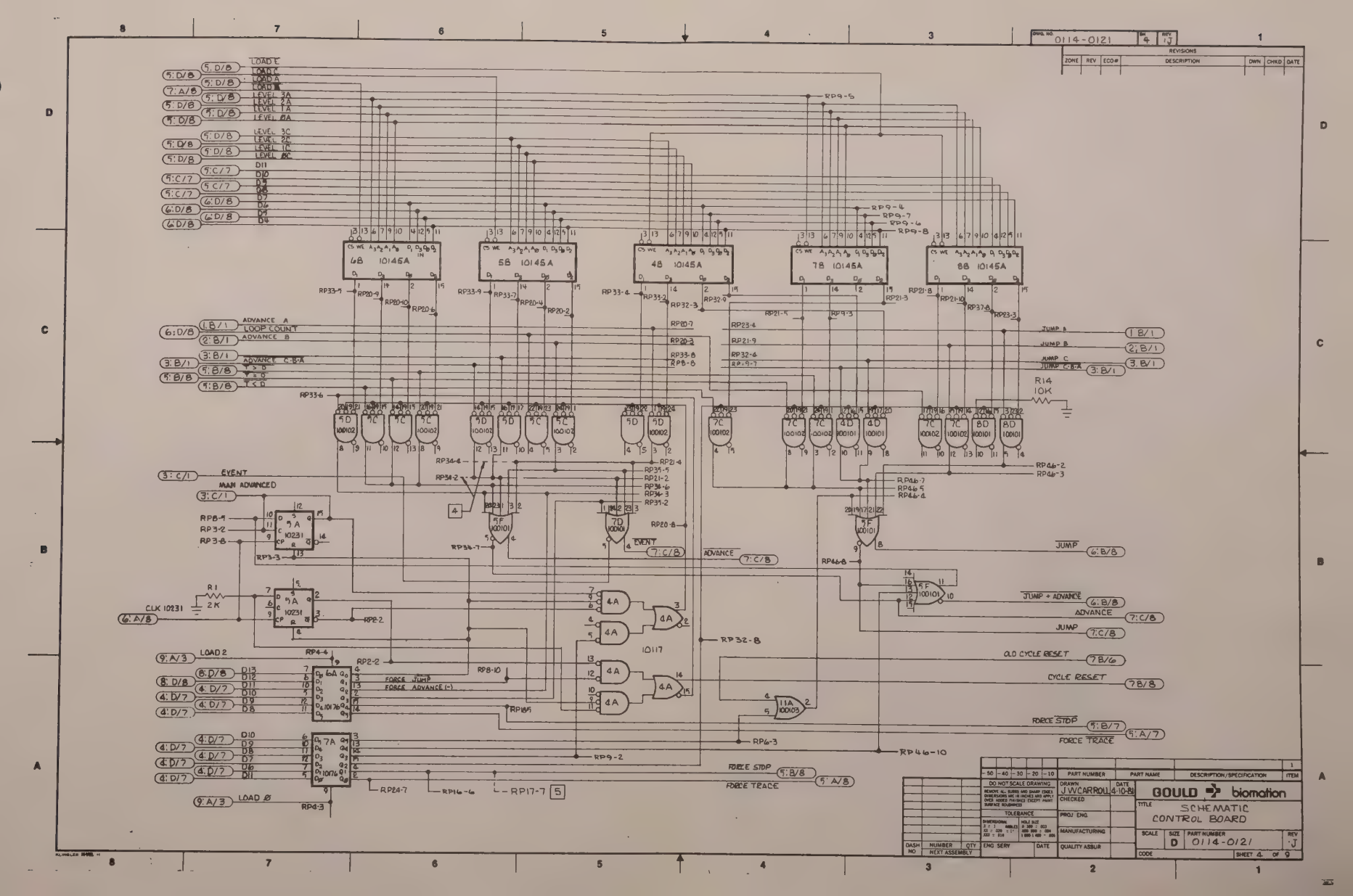
DASH NO. | NUMBER | QTY | NEXT ASSEMBLY | ENG SERV. K. Higgins | DATE 1/7/82

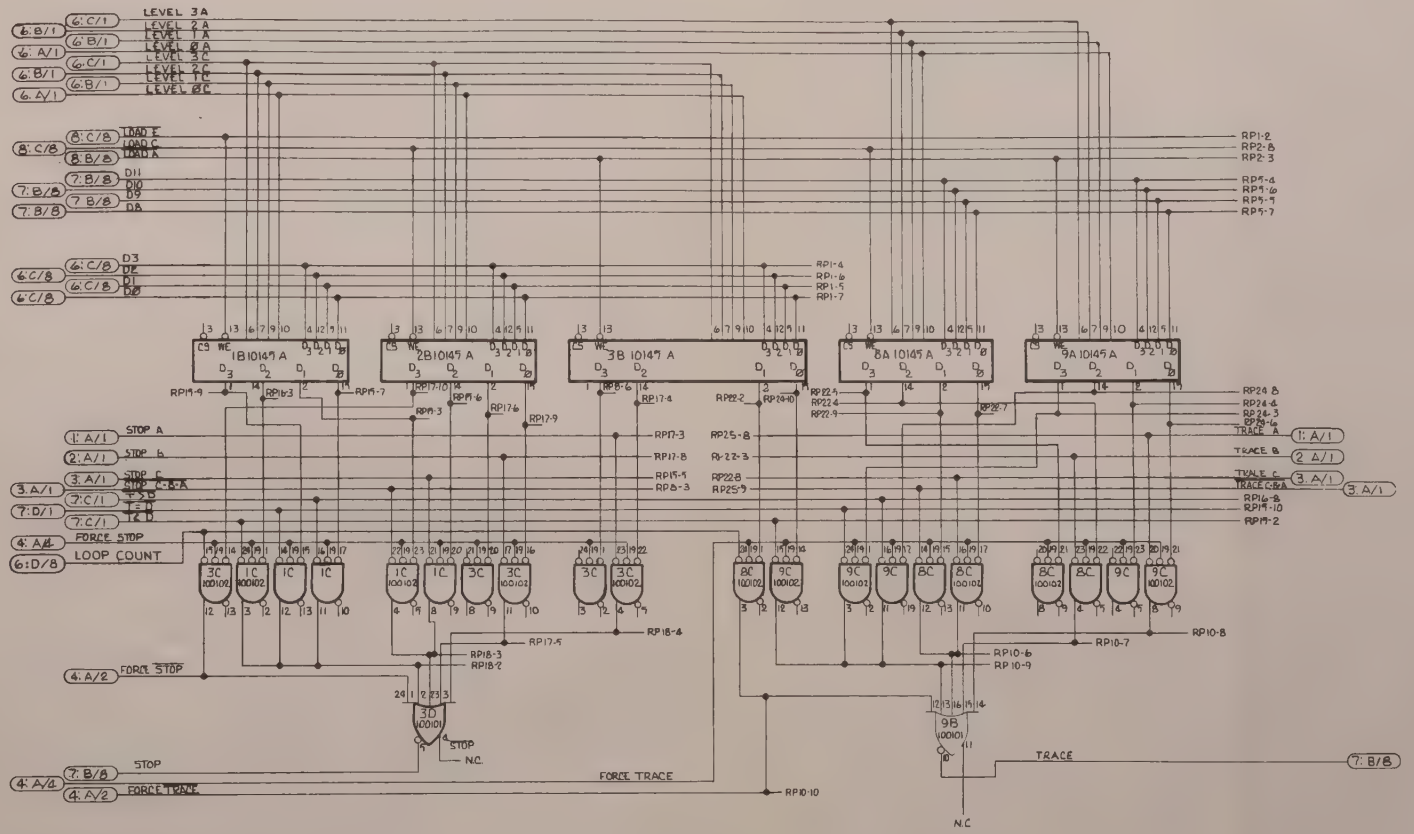


DWG NO 0114-0121
SH 2
REV J
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
CLK176A
CLK176B
3H 4H 10176
4H 10176
6H 10176
6H 7H 10176
LEVEL 0D
LEVEL 1D
LEVEL 2D
LEVEL 3D
LEVEL 0C
LEVEL 1C
LEVEL 2C
LEVEL 3C
LEVEL 0B
LEVEL 1B
LEVEL 2B
LEVEL 3B
LEVEL 0A
LEVEL 1A
LEVEL 2A
LEVEL 3A
D7
D6
D5
D4
LOAD 6
BD11
READ
A3
A2
A1
ADDRESS
D IN
D OUT
SELECT
10422 4G
10422 4F
10422 7G
10422 7F
SELECT F-C
SELECT 7-4
SELECT B-8
SELECT 3-0
ADVANCE C-B-A
ADVANCE B
JUMP C-B-A
JUMP B
STOP C-B-A
STOP B
TRACE C-B-A
TRACE B
10164
RP73-2
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC CONTROL BOARD (10422)
SCALE
SIZE D
PART NUMBER 0114-0121
REV J
CODE K101-D
SHEET 2 OF 9
DASH NO.
NUMBER
QTY
NEXT ASSEMBLY



DWG. NO 0114-0121
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
CLK 176A
1H 10176
2H 10176
3H 10176
10176 2J
10422 1G
10422 1F
10422 3G
10422 3F
10164
LEVEL 3D
LEVEL 2D
LEVEL 1D
LEVEL ØD
LEVEL 3C
LEVEL 2C
LEVEL 1C
LEVEL ØC
LOAD 6
SELECT F-C
SELECT 7-4
SELECT B-8
SELECT 3-Ø
FORCE LEVEL = Ø
BD10
READ
EVENT
STOPPED
ADVANCED ENDED
MAN ADVANCED
ECL DIN Ø
ADVANCE C·B·A
ADVANCE C
JUMP C·B·A
JUMP C
STOP C·B·A
STOP C
TRACE C·B·A
TRACE C
R13 68Ω
-2.0V
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC CONTROL BOARD (10422)
SCALE
SIZE D
PART NUMBER 0114-0121
REV J
CODE K101 D
SHEET 3 OF 9


DWG. NO. 0114-0121
REV. J
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
LOAD E
LOAD D
LOAD A
LOAD B
LEVEL 3A
LEVEL 2A
LEVEL 1A
LEVEL ØA
LEVEL 3C
LEVEL 2C
LEVEL 1C
LEVEL ØC
D11
D10
D9
D8
D7
D6
D5
D4
6B 10145A
5B 10145A
4B 10145A
7B 10145A
8B 10145A
ADVANCE A
LOOP COUNT
ADVANCE B
ADVANCE C-B-A
EVENT
MAIN ADVANCED
CLK 10231
LOAD 2
LOAD Ø
FORCE JUMP
FORCE ADVANCE (-)
10117
JUMP A
JUMP B
JUMP C
JUMP C-B-A
R14 10K
JUMP
JUMP + ADVANCE
ADVANCE
JUMP
OLD CYCLE RESET
CYCLE RESET
FORCE STOP
FORCE TRACE
PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITEM
DO NOT SCALE DRAWING
DRAWN J.W.CARROLL 4-10-81
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV
DASH NO. | NUMBER | QTY | NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC CONTROL BOARD
SCALE | SIZE D | PART NUMBER 0114-0121 | REV J
CODE | SHEET 4 OF 9



DASH NO	NUMBER NEXT ASSEMBLY	QTY
	ENG SERV	DATE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING

TOLERANCE

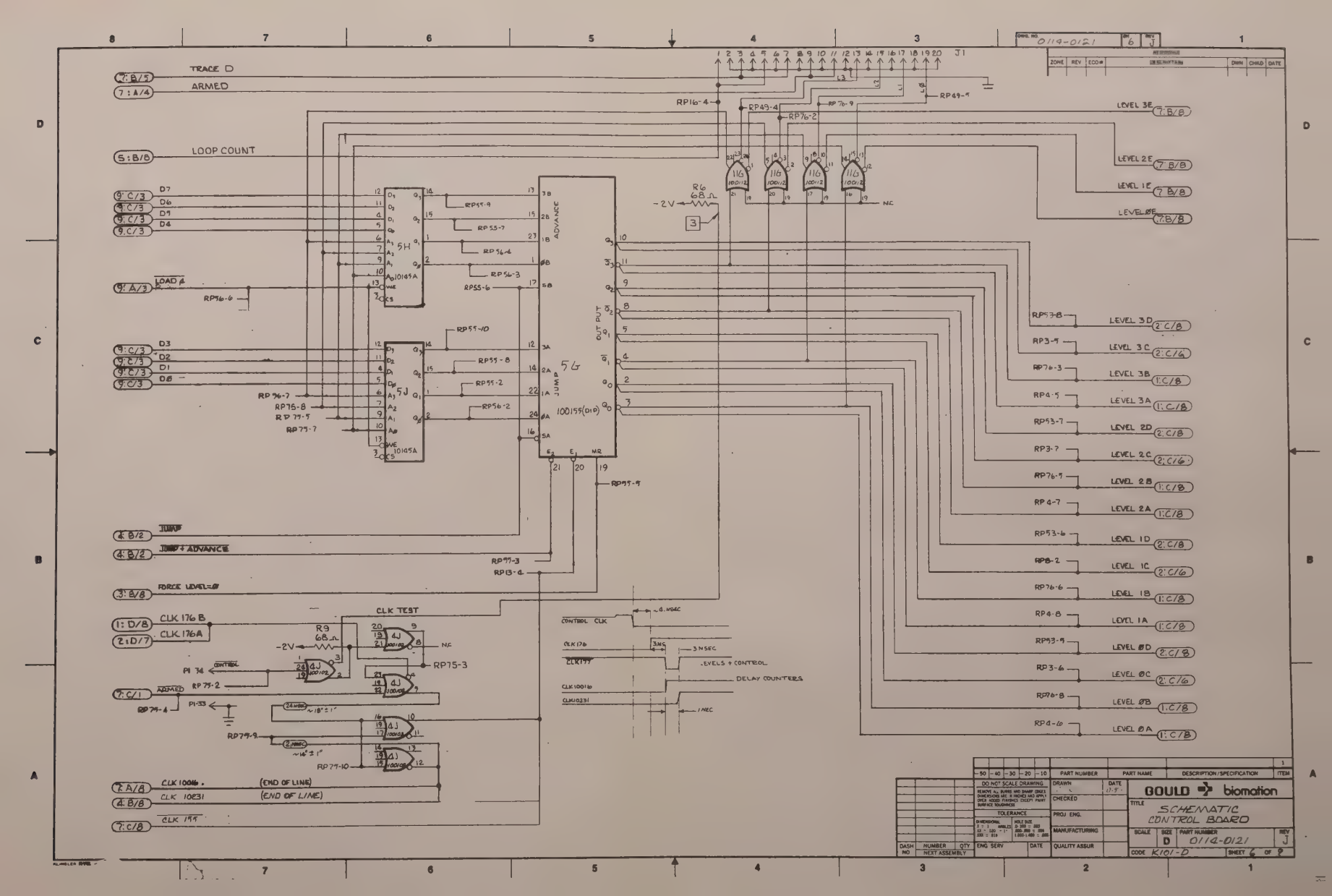
DRAWN: J.W.CARROLL 4-2-81
CHECKED:
PROJ. ENG.:
MANUFACTURING:
QUALITY ASSUR:

GOULD biomation

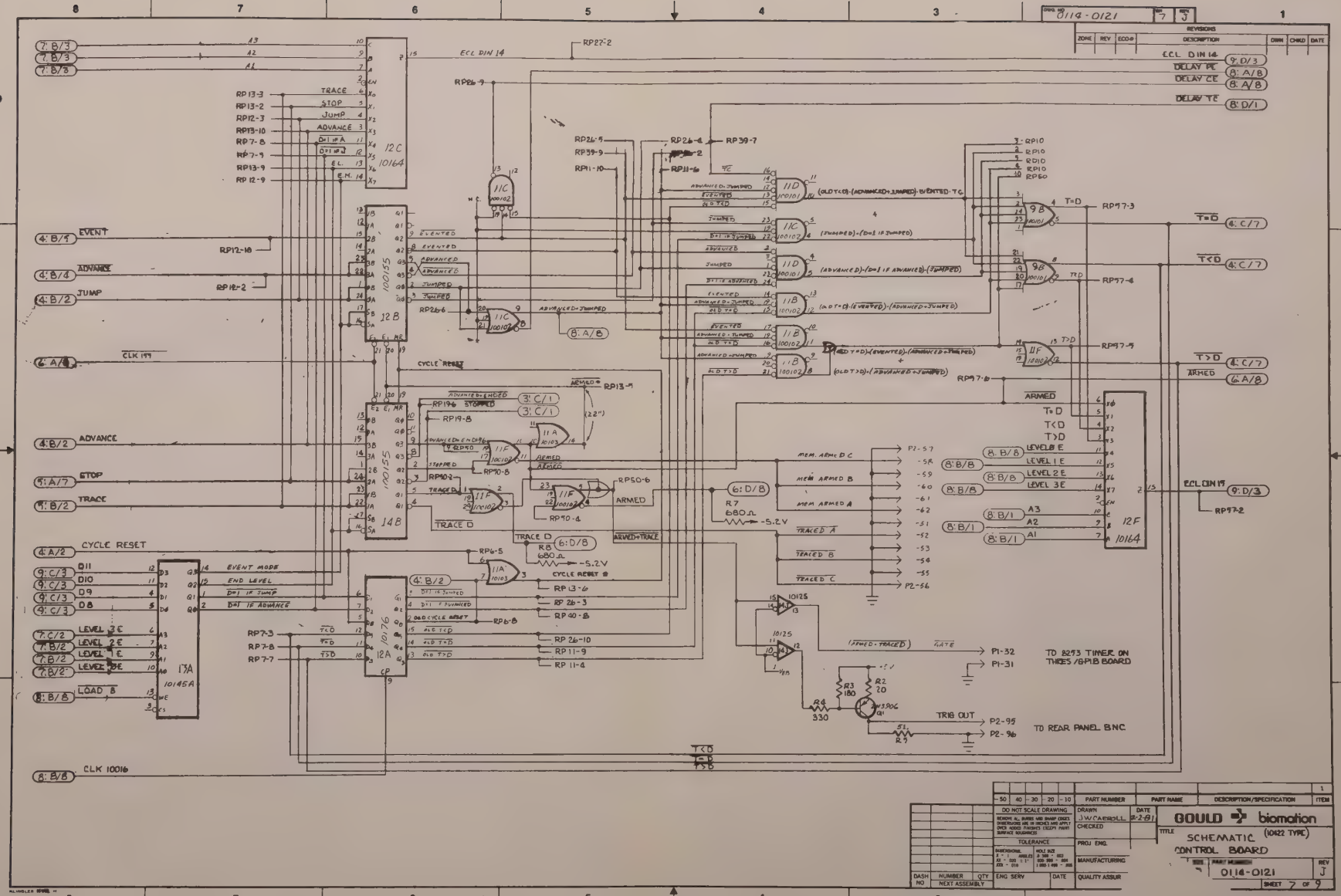
TITLE: SCHEMATIC CONTROL BOARD

SCALE: | SIZE: D | PART NUMBER: 0114-0121 | REV: J

CODE: K1010 | SHEET 5 OF 9



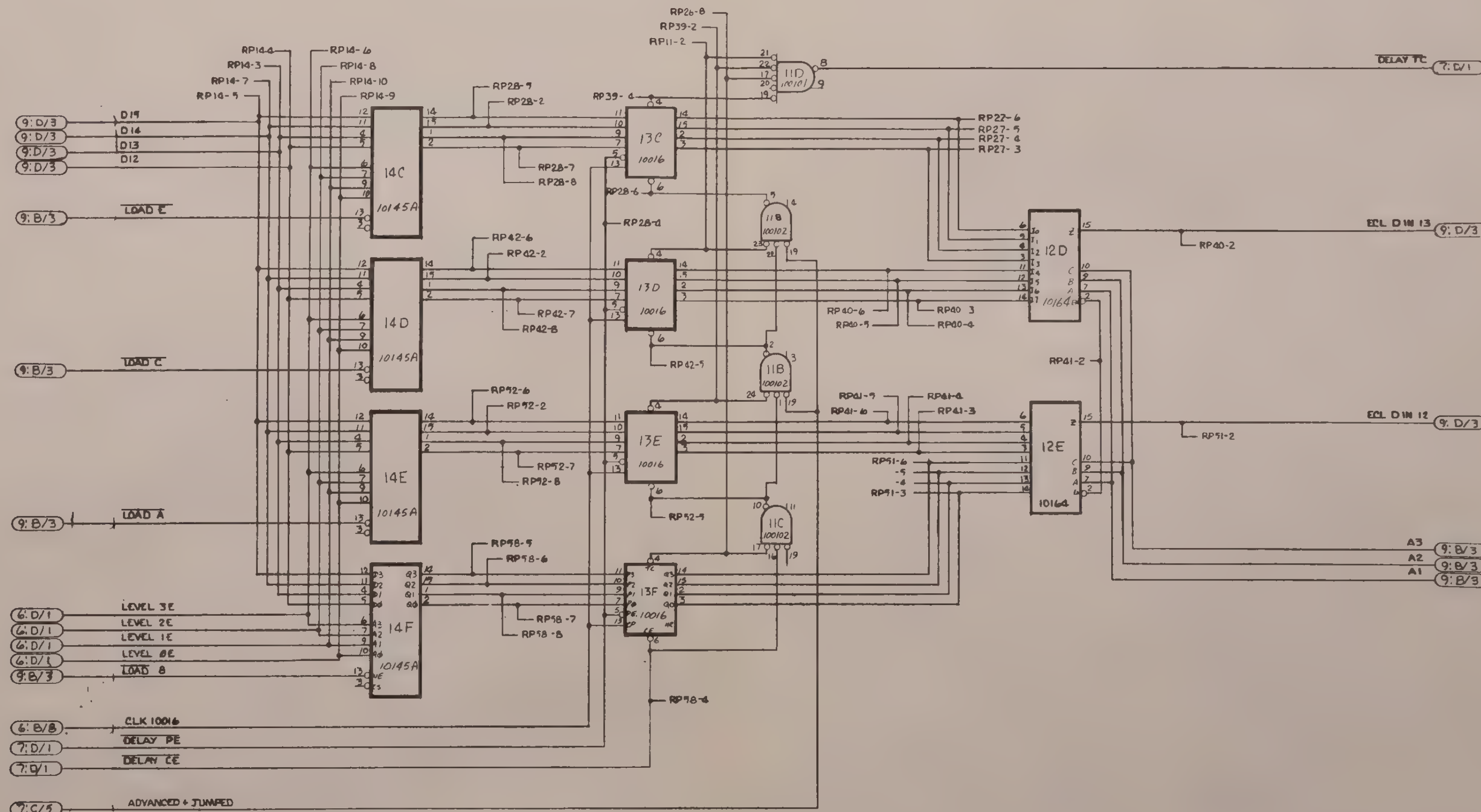
DWG. NO. 0114-0121
SH 6
REV J
TRACE D
ARMED
LOOP COUNT
LOAD 4
JUMP
JUMP + ADVANCE
FORCE LEVEL=Ø
CLK 176 B
CLK 176A
CLK TEST
CLK 10016
CLK 10231
CLK 155
(END OF LINE)
(END OF LINE)
5H
5J
5G
10145A
100155(DIP)
ADVANCE
JUMP
OUT PUT
LEVEL 3E
LEVEL 2E
LEVEL 1E
LEVEL ØE
LEVEL 3D
LEVEL 3C
LEVEL 3B
LEVEL 3A
LEVEL 2D
LEVEL 2C
LEVEL 2B
LEVEL 2A
LEVEL 1D
LEVEL 1C
LEVEL 1B
LEVEL 1A
LEVEL ØD
LEVEL ØC
LEVEL ØB
LEVEL ØA
CONTROL CLK
CLK176
CLK177
CLK10016
CLK10231
LEVELS + CONTROL
DELAY COUNTERS
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
SCHEMATIC
CONTROL BOARD
SCALE
SIZE D
PART NUMBER 0114-0121
REV J
CODE K101-D
SHEET 6 OF 9



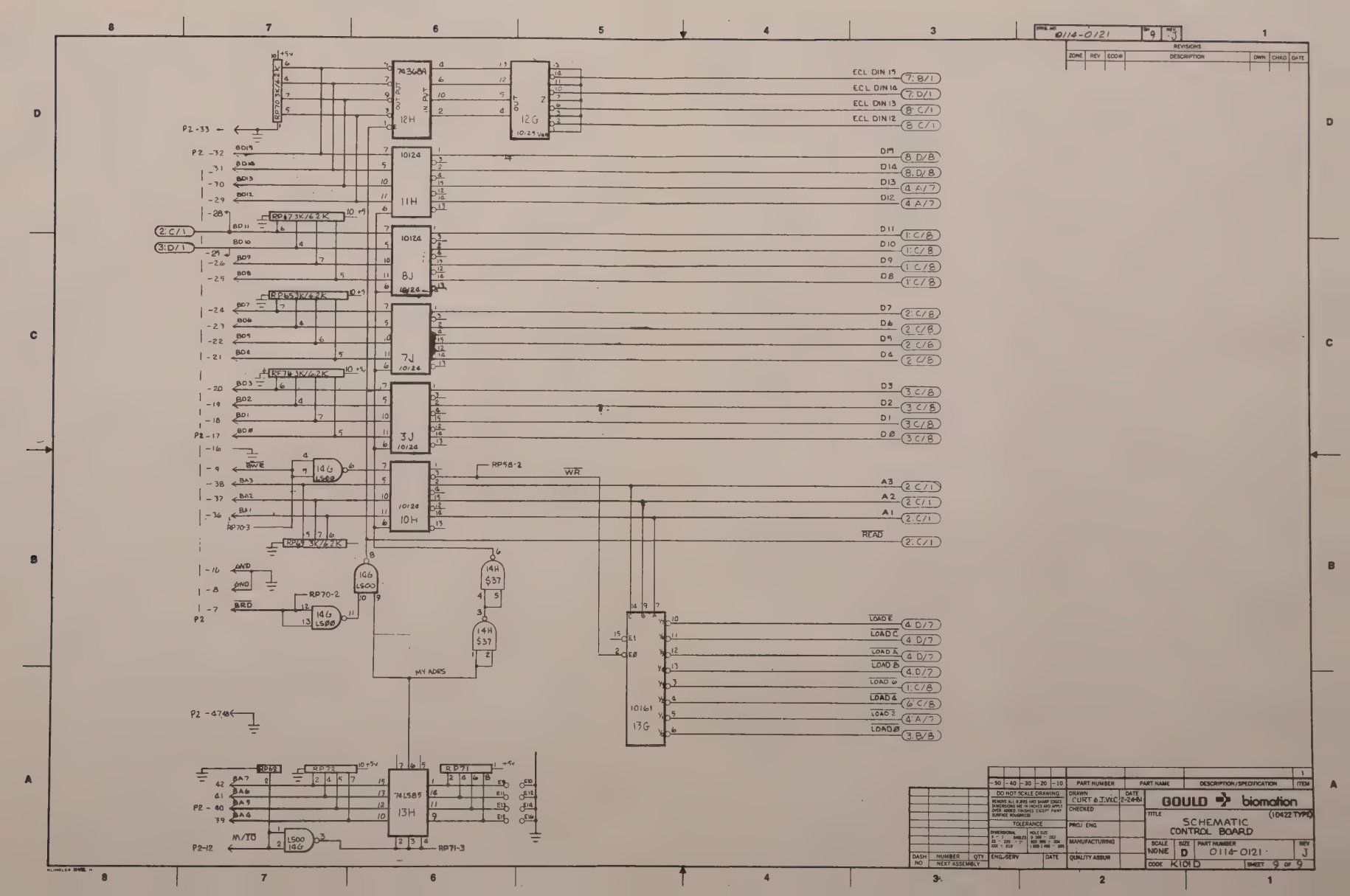
0114-0121
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
ECL DIN 14
DELAY PE
DELAY CE
DELAY TC
EVENT
ADVANCE
JUMP
CLK 159
CYCLE RESET
STOP
TRACE
CYCLE RESET
D11
D10
D9
D8
LEVEL 3E
LEVEL 2E
LEVEL 1E
LEVEL 3E
LOAD 8
CLK 10016
EVENT MODE
END LEVEL
D=1 IF JUMP
D=1 IF ADVANCE
ARMED
ARMED+TRACE
TRACE D
MEM. ARMED C
MEM ARMED B
MEM ARMED A
TRACED A
TRACED B
TRACED C
LEVEL 3E
LEVEL 1E
LEVEL 2E
LEVEL 3E
ECL DIN 15
TO 8253 TIMER ON THRESS/GPIB BOARD
TRIG OUT
TO REAR PANEL BNC
GATE
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
J.W.CARROLL
DATE
2-2-81
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC (10422 TYPE)
CONTROL BOARD
0114-0121
REV
J
SHEET 7 OF 9

DWG. NO. 0114 0121 | SH 8 | REV J

ZONE	REV	ECO#	REVISIONS DESCRIPTION	DWN	CHKD	DATE



DO NOT SCALE DRAWING	DRAWN WCARROLL	DATE	GOULD biomation
TOLERANCE	CHECKED		TITLE SCHEMATIC CONTROL BOARD
	PROJ. ENG.		SCALE — SIZE D PART NUMBER 0114 0121 REV J
ENG. SERV DATE	MANUFACTURING / QUALITY ASSUR		CODE K101-D SHEET 8 OF 9



0114-0121
9
J
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
74368A
12H
12G
10.25 Vdc
10124
11H
8J
7J
3J
10H
14G
LS00
14H
$37
10161
13G
74LS85
13H
RP70 3K/6.2K
RP67 3K/6.2K
RP65 3K/6.2K
RP74 3K/6.2K
RP69 3K/6.2K
RP70-2
RP70-3
RP58-2
RP71-3
RP69
RP72
RP71
MY ADRS
WR
READ
ECL DIN 15
ECL DIN 14
ECL DIN 13
ECL DIN 12
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
A3
A2
A1
LOAD E
LOAD C
LOAD A
LOAD B
LOAD 6
LOAD 4
LOAD 2
LOAD 0
P2-33
P2-47,48
P2-12
M/IO
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CURT & J.W.C
DATE
2-24-81
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG-SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
SCHEMATIC
CONTROL BOARD
(10422 TYPE)
SCALE
NONE
SIZE
D
PART NUMBER
0114-0121
REV
J
CODE
K101D
SHEET
9 OF 9

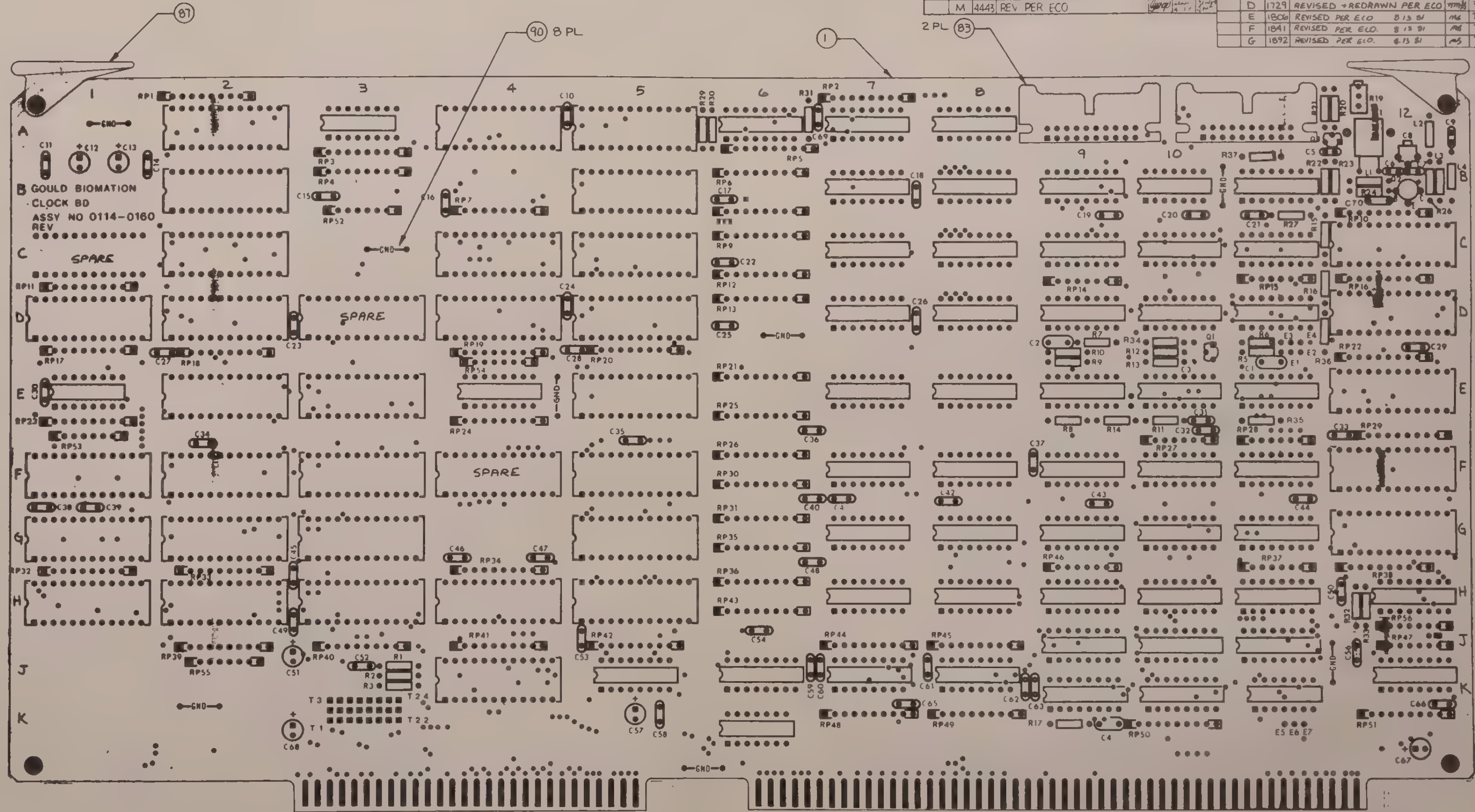
DWG NO 0114-0160 SH 1 REV M

G		PROD REL ERN # 207		RG		
H	3641	REV'D PER ECO	MW			
J	3573	REV'D PER ECO				
K	4214	REV D PER ECO				
L	4179	REVISED PER ECO	D C			
M	4443	REV PER ECO				

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—				
	B		REL TO PILOT RUN ERN 0130	4/9/81	JL	
	C	1685	REVISED PER ECO 6-24-81	JWC	RD	
	D	1729	REVISED + REDRAWN PER ECO		RD	
	E	1806	REVISED PER ECO 8 13 81	MS	RD	
	F	1841	REVISED PER ECO. 8 13 81	MS	RD	
	G	1892	REVISED PER ECO. 8 13 81	MS	RD	

MRC 4634 PER ECO



-10	0114-0002	1
DASH NO	NUMBER / NEXT ASSEMBLY	QTY

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL	HOLE SIZE
X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010	0-.399 ± .003 .400-.999 ± .004 1.000-1.499 ± .005

ENG SERV: R. Lowe DATE 1/7/82

DRAWN	N.M. Grilli	6/26/81
CHECKED	K. Doan	1/22/82
PROJ ENG		1/7/82
MANUFACTURING		1/7/82
QUALITY ASSUR		1/7/82

GOULD biomation

TITLE: ASSEMBLY — CLOCK PWB

SCALE	SIZE	PART NUMBER	REV
2/1	D	0114-0160	M

CODE K101-D SHEET 1 OF 1

COMMENTS	TOTAL COST	UNIT COST
-10 = K205-48 CH		
-20 = K205-32 CH		

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1					1	1	0114-0162	PWB				FAB
2												
3					2	2	1400-0019	TRANSISTOR	Q1, Q3		2N3906	
4					5	5	3000-1200	RESISTOR	R1-3, R34, R37		120Ω 1/4W 5%	
5					1	1	1300 0038	TRANSISTOR	Q2		BFR 91	
6												
7					1	1	1800-0105	I.C.	11K		74LS00	
8					1	1	1800-0254	I.C.	12J		74LS85	
9					1	1	1800-0349	I.C.	9F		74368A	
10					1	1	1800-0280	IC	6K		74 S37	
11					1	1	1820-0028	I.C.	9B		4028	
12					1	1	1820-0065	I.C.	10B		4069	
13					2	2	1820-0063	I.C.	9C, 9D		14518	
14												
15					7	7	1850-0077	I.C.	1D, 2H, 4C, 4D,		100101	
16									4H, 4J 12E			
17					1	1	6100-0119	SOCKET	X6K		14 PIN	
18												

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROTOTYPE	4/8/81	MB		
B	RELEASE TO PILOT RUN ERN# 0130	4/9/81	MB	JL	
C	REVISED PER ECO # 1689	6/26/81	MB	RD	
D	REVISED PER ECO # 1729	6/27/81	MB	RD	
E	REVISED PER ECO # 1806	8/14/81	MB	RD	
F	REVISED PER ECO # 1841	8/19/81	MB	RD	
G	REVISED PER ECO # 1892	6/14/81	MB	RD	

DRAWN	DATE
M Bruce	3.9.81
CHECKED R Dean	4/5/82
ENGINEER	1.7.82
MANUFACTURING	1/7/82
QUALITY ASSURANCE	1/7/82

DASH NO.	NUMBER	QTY
-10	0114-0002	1
	NEXT ASSEMBLY	

LIST OF MATERIAL

ASSY, CLOCK PWB

biomation

REV	
B	0114-0160 M

MODEL K101-D | CODE | SHEET 1 OF 5

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	20	10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19					25	25	1850-0078	I.C.	2A thru 2G, 12C,	12D, 4A	100102	
20					—	—			5A thru 5H, 3E thru 3H, 1F, 1G, 1H			
21					2	2	1850-0088	I.C.	12F, 12G		10422	
22					4	4	1850-0094	I.C.	1E, 4E, 3A, 6A		10216	
23					2	2	1850-0097	I.C.	5J, 11D,		10231	
24					22	22	1850-0098	I.C.	7A thru 7H, 9G, 11E, 9H, 10J		10176	
25					—	—			8A thru 8H, 10H, 11F			
26					2	2	1850-0105	I.C.	10G, 11J		10173	
27					1	1	1850-0099	I.C.	10C		10164	
28					1	1	1850-0100	I.C.	9J		10161	
29					2	2	1850-0101	I.C.	9E, 10E		10137	
30					1	1	1850-0103	I.C.	10F		10125	
31					5	5	1850-0104	I.C.	6J, 7J, 8J, 9K, 10K		10124	
32					1	1	1850-0108	I.C.	10D		10109	
33					2	2	1850-0113	I.C.	11H, 11C,		10101	
34					3	3	1850-0114	I.C.	11B, 11G, 12H		10016	
35					2	2	6100-0137	SOCKET	12F, 12G		24 PIN	
36					2	2	2100-0014	INDUCTOR	L2, L3		.1 mh	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	PROD REL PER ERN #0207	1/9/82	MB	RD	
H	REV'D PER ECO # 3641	11/18/83	ITW	DWG	4/7/83
J	REV'D PER ECO 4073	8/30/83	MB	RD	
K	REVISED PER ECO 4214	1/18/84	DC		
L	REVISED PER ECO 4179	2/17/84	P.C		
M	PER ECO # 4443	9/6/84			
MRC	PER ECO # 4634	7-9-84			

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

LIST OF MATERIAL

ASSY, CLOCK PWB

biomation

REV	
B	0114-0160 M

MODEL K101-D | CODE | SHEET 2 OF 5

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37					1	1	2100-0012	INDUCTOR	L1		.47uh	
38					1	1	2100-0036	INDUCTOR	L4		SHIELD BEAD	
39												
40					1	1	2950-5106	RESISTOR	R24		51Ω 1/8W 5%	
41					2	2	3000-1000		R35, R36		100Ω 1/4W 5%	
42					1	1	3000-8200		R21		820Ω 1/4W 5%	
43					1	1	-1006		R9		10Ω 1/4W 5%	
44					1	1	-1501		R26		1.5K 1/4W 5%	
45					1	1	-1600		R15		160Ω 1/4W 5%	
46					1	1	-1800		R16		180Ω 1/4W 5%	
47												
48					3	3	-2001		R8, R7, 32		2K 1/4W 5%	
49					4	4	-2200		R10, 12, 20, 23		220Ω 1/4W 5%	
50												
51					1	1	-3006		R5		30Ω 1/4W 5%	
52					1	1	-4700		R13		470Ω 1/4W 5%	
53					1	1	-5100		R27		510Ω 1/4W 5%	
54					1	1	3000-5600	RESISTOR	R22		560Ω 1/4W 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO. | NUMBER NEXT ASSEMBLY | QTY

LIST OF MATERIAL

ASSY, CLOCK PWB

MODEL K101-D

biomation

B | 0114-0160 | REV M

CODE | SHEET 3 OF 5

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55					1	1	3000-3001	RESISTOR	R33		3K 1/4W 5%	
56					1	1	3000-6800	RESISTOR	R6		680Ω 1/4W 5%	
57					3	3	3000-6806	RESISTOR	R11, 14, 17		68Ω 1/4W 5%	
58					3	3	3000-2201	RESISTOR	R29, 30, 31		2.2K 1/4W 5%	
59					1	1	3300-0067	POT	R19		200Ω	
60					1	1	3700-0051	RES PAK	RP14		10K 8PIN	SIP
61					4	4	-0049		RP48-51		3K/6.2K 10 PIN	SIP
62					4	4	-0057		RP47, 52, 53, 54		2.2K 8 PIN	SIP
63					4	4	-0039-10		RP3, 5, 23, 24		56Ω 10 PIN	SIP
64					6	6	3700-0091	RES PAK	RP15, 27, 28, 37, 46, 56		68Ω 8 PIN	
65												
66					36	36	3700-0092	RES PAK	RP1 2, 4, 6-13, 16-22		68Ω 10 PIN	SIP
67					—	—	-		25, 26, 29-36, 38-45			
68					1	1	5100-0004	CRYSTAL	Y1		100 MHz	
69					1	1	3700-0096	RES PAK	RP55		100Ω 8PIN 7RES	
70					1	1	4010-0330	CAPACITOR	C70		33pf	
71					1	1	4010-0680	CAPACITOR	C1,		68 PF	
72												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

DASH NO | NUMBER NEXT ASSEMBLY | QTY

LIST OF MATERIAL

ASSY, CLOCK PWB

MODEL K101-D

biomation

B | 0114-0160 | REV M

CODE | SHEET 4 OF 5

COMMENTS		TOTAL COST	UNIT COST
-10 = K205 -48 CH			
-20 = K205 -32 CH			

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
73					1	1	4010-5606	CAPACITOR	C7		5.6PF	
74												
75												
76					57	57	4010-0103	CAPACITOR	C2,4-6,9-11,14-50		.01 mf	1 SM.
77									52-54,56,58-63,65,66,69			
78												
79					6	6	4400-0043	CAPACITOR	C12,13,51,57,67,68		47mf/6V ALUM.	
80					1	1	4600-0009	VAR. CAP	C8		1.25-3 PF	
81					8	—	6000-0571-10	CONN.	-20 T2-T3, T5-T6, T8 T9, T17-T18, T20-T21	T11-T12, T14-T15 T23-T24	SHORTING	
82					—	8	6000-0571-10		-10 T1-T2 T4-T5, T7-T8-T14, T16-T17, T19-	T8, T10-T11 T20 T22-T25	PLUG	
83					2	2	6000-0384	HEADER	J1, J2		20 PIN RT ANGLE	
84					3	3	6000-0293-8	HEADER			SINGLE ROW 8 POS.	
85					2	2	6100-0137	SOCKET	12F, 12G		24 PIN .4"	
86												
87					1	1	0112-0228-05	EJECTOR	A5			
88					1	1	7000-0120	EJECTOR HANDLE				
89												
90					8	8	9000-0054	GND BUSS				FAB

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DRAWN	DATE
	CHECKED	
	ENGINEER	
	MANUFACTURING	
	QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY, CLOCK PWB

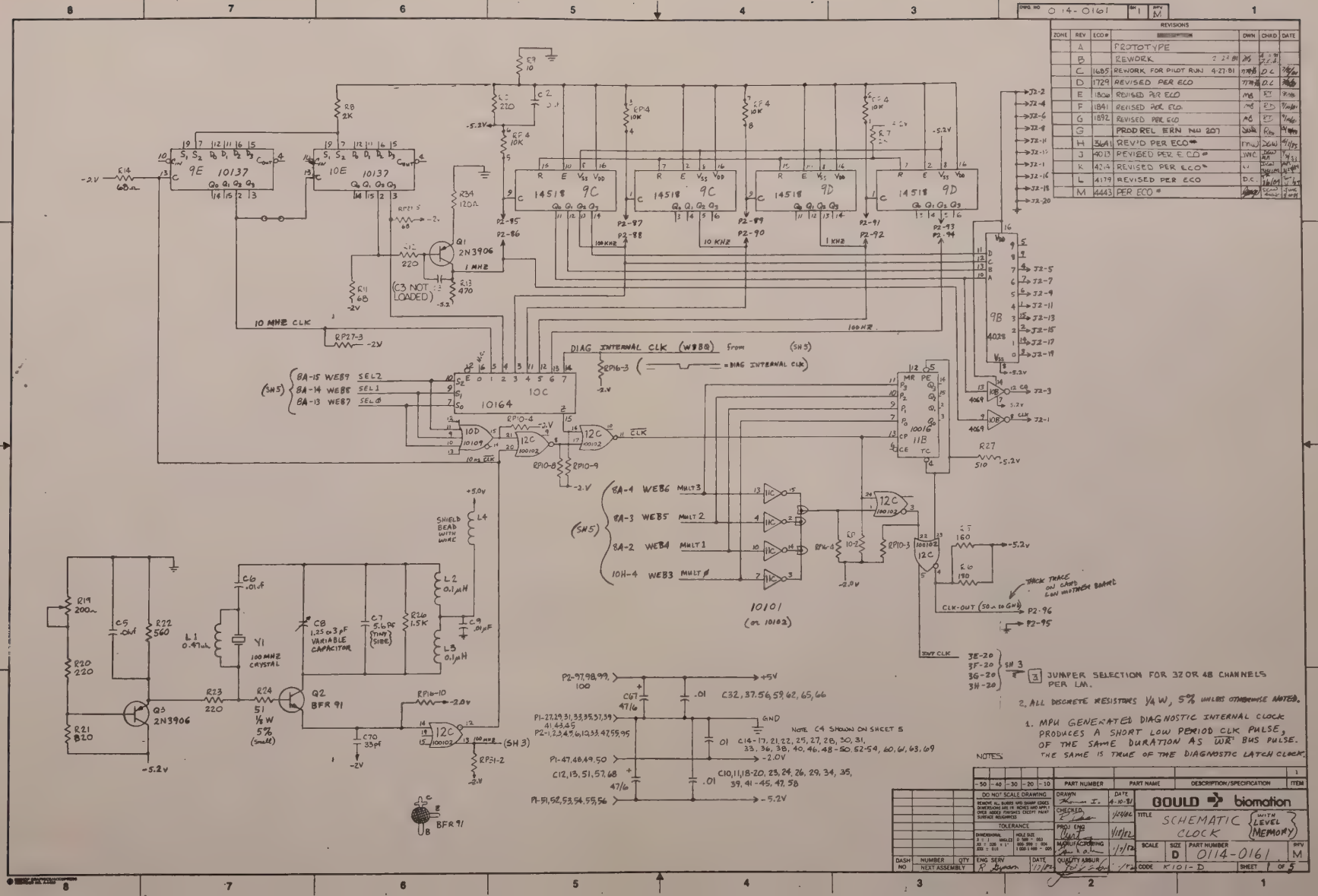
MODEL K101-D

biomation

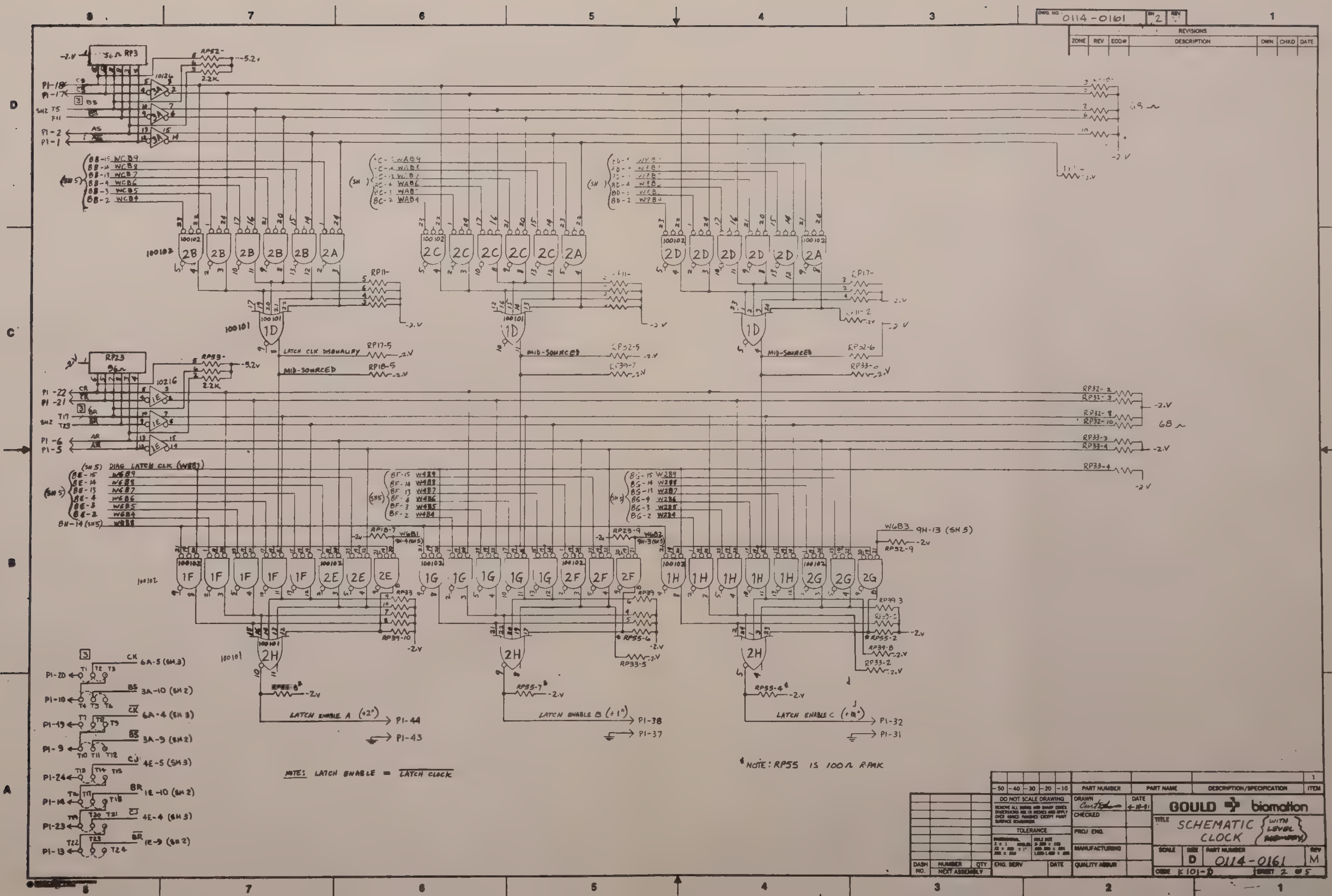
B 0114-0160 REV M

CODE

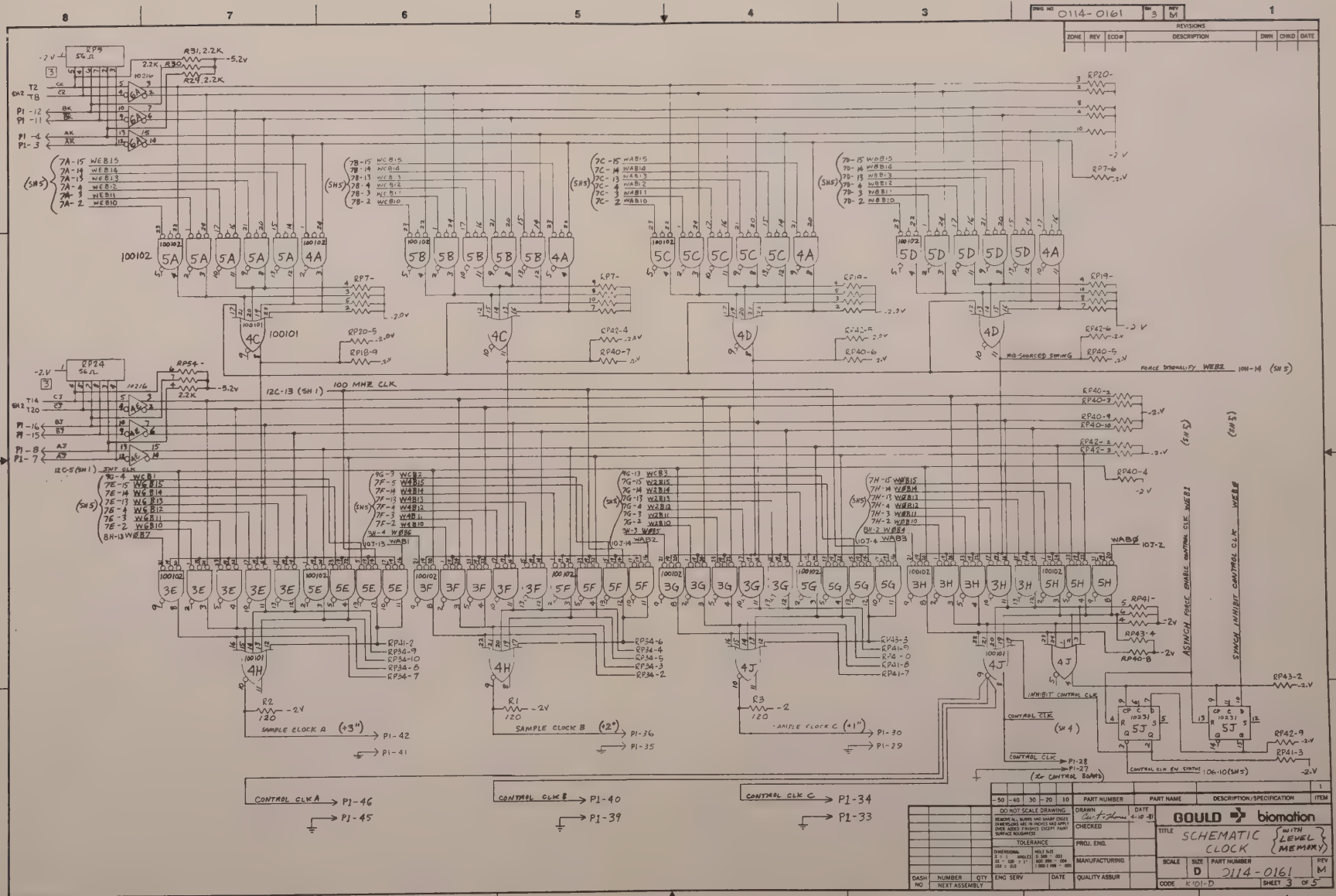
SHEET 5 OF 5

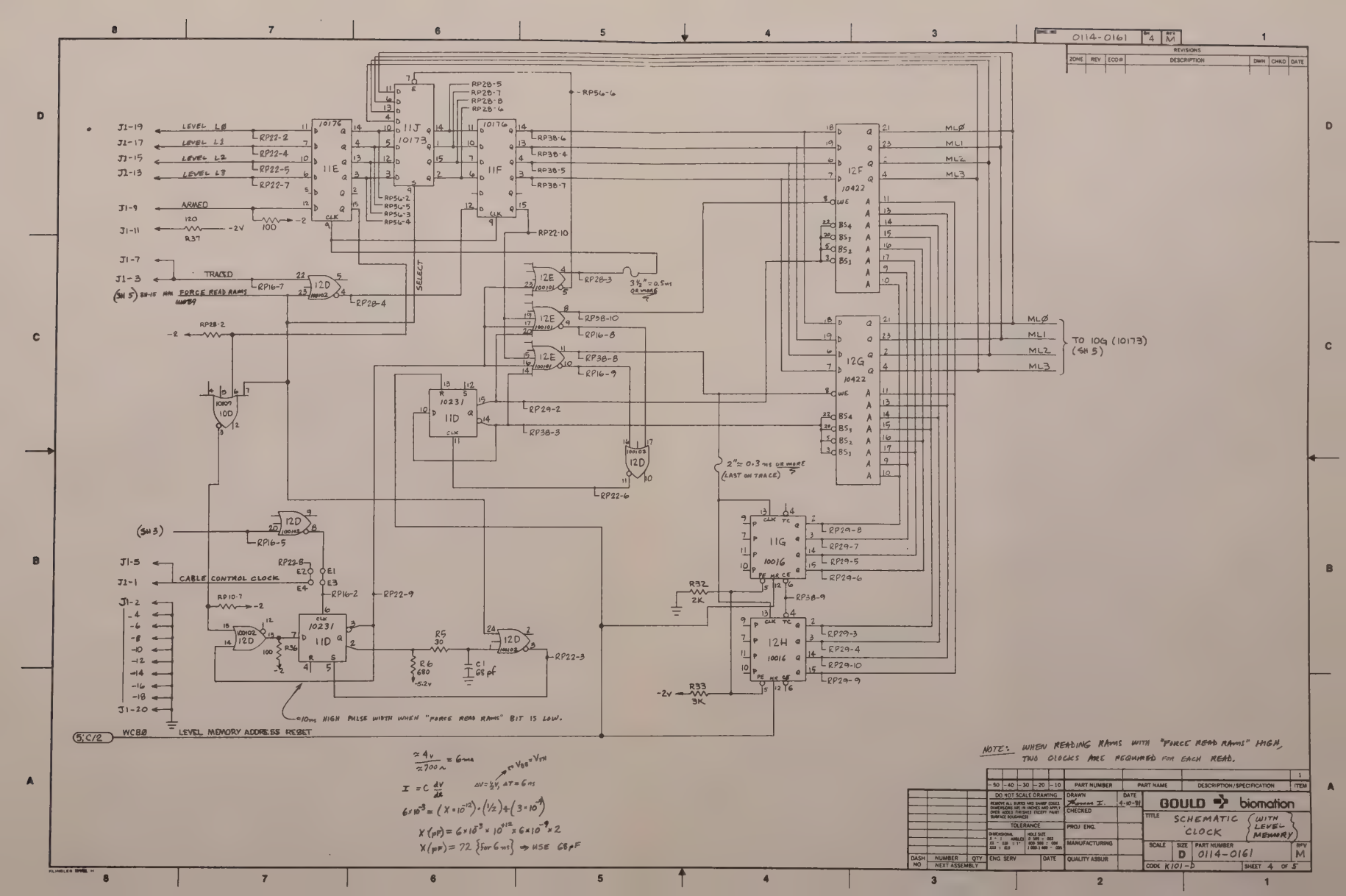


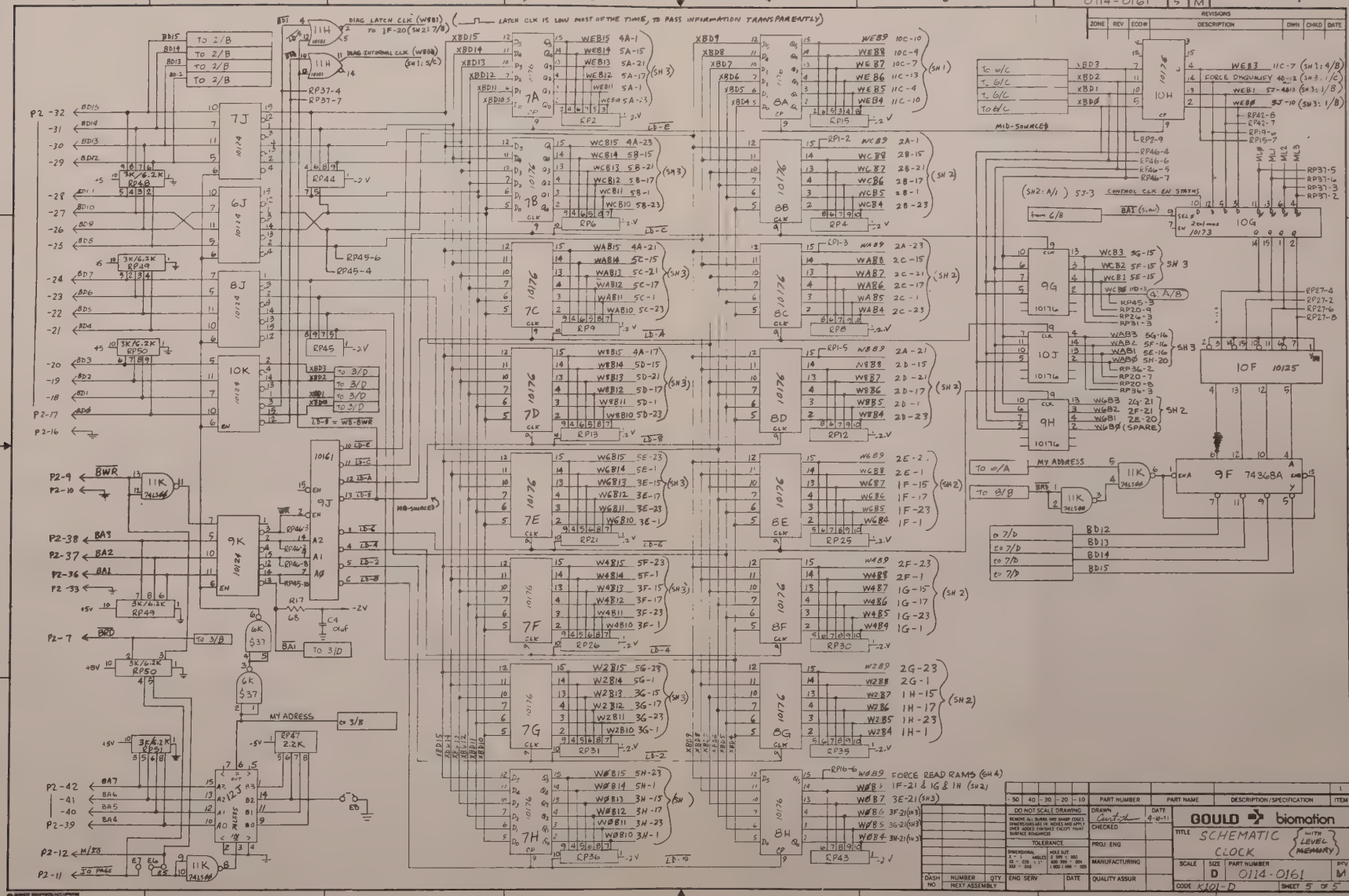
DWG NO 0114-0161
SH 1
REV M
REVISIONS
ZONE | REV | ECO# | DWN | CHKD | DATE
A | PROTOTYPE
B | REWORK 2-27-81
C | 1685 | REWORK FOR PILOT RUN 4-27-81
D | 1729 | REVISED PER ECO
E | 1806 | REVISED PER ECO
F | 1841 | REVISED PER ECO
G | 1892 | REVISED PER ECO
G | PROD REL ERN NO 207
H | 3641 | REV'D PER ECO#
J | 4013 | REVISED PER ECO#
K | 4214 | REVISED PER ECO#
L | 4179 | REVISED PER ECO
M | 4443 | PER ECO#
9E 10137
10E 10137
14518 9C
14518 9C
14518 9D
14518 9D
Q1 2N3906
(C3 NOT LOADED)
10 MHZ CLK
DIAG INTERNAL CLK (W8BQ) from (SH5)
= DIAG INTERNAL CLK
10164 10C
10109 10D
10016 11B
9B 4028
8A-15 WEB9 SEL2
8A-14 WEB8 SEL1
8A-13 WEB7 SEL0
8A-4 WEB6 MULT3
8A-3 WEB5 MULT2
8A-2 WEB4 MULT1
10H-4 WEB3 MULT0
10101 (or 10102)
SHIELD BEAD WITH WIRE
L4
Y1 100 MHZ CRYSTAL
C8 1.25 to 3 pF VARIABLE CAPACITOR
C7 5.6 pF (TINY SIZE)
Q2 BFR 91
Q3 2N3906
BFR 91
THICK TRACE ON CARD LOW MOTHER BOARD
CLK-OUT (50 Ω to GND)
INT CLK
3E-20
3F-20
3G-20
3H-20
SH 3
3 JUMPER SELECTION FOR 32 OR 48 CHANNELS PER LM.
2. ALL DISCRETE RESISTORS 1/4 W, 5% UNLESS OTHERWISE NOTED.
1. MPU GENERATED DIAGNOSTIC INTERNAL CLOCK PRODUCES A SHORT LOW PERIOD CLK PULSE, OF THE SAME DURATION AS WR BUS PULSE. THE SAME IS TRUE OF THE DIAGNOSTIC LATCH CLOCK.
NOTES:
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)
SCALE
SIZE D
PART NUMBER 0114-0161
REV M
CODE K101-D
SHEET 1 OF 5



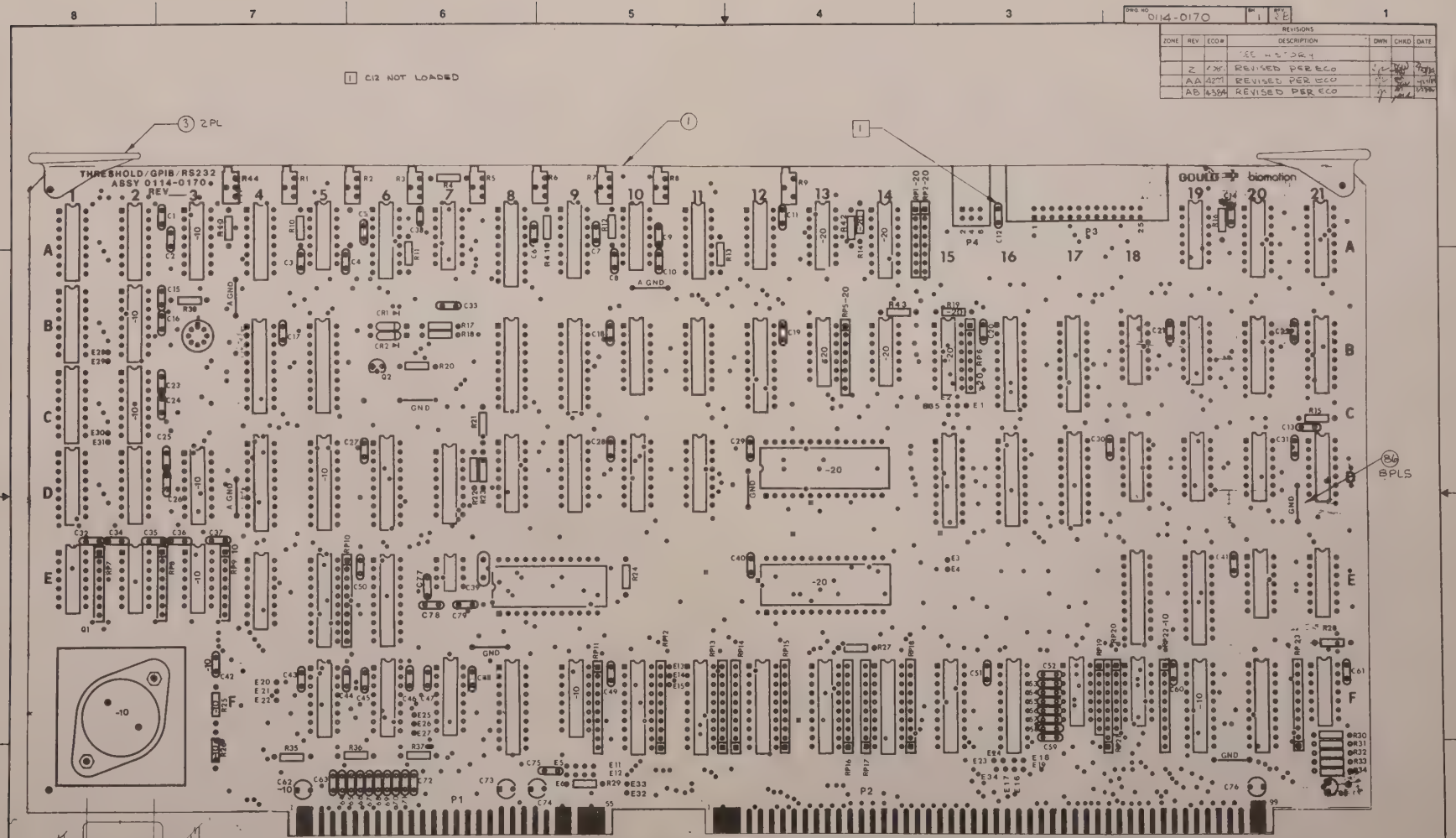
0114-0161
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
LATCH CLK DISQUALIFY
MID-SOURCED
DIAG LATCH CLK (W6B8)
LATCH ENABLE A (+2°) → P1-44
P1-43
LATCH ENABLE B (+1°) → P1-38
P1-37
LATCH ENABLE C (+0°) → P1-32
P1-31
NOTE: LATCH ENABLE = LATCH CLOCK
* NOTE: RP55 IS 100Ω R-PAK
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV
DASH NO.
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)
SCALE
SIZE D
PART NUMBER 0114-0161
REV M
CODE K101-D
SHEET 2 OF 5


DWG NO 0114-0161
REV M
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
RP8 56Ω
R31, 2.2K
R30 2.2K
R29, 2.2K
-5.2v
-2v
100102
100101
5A 5B 5C 5D 4A 4C 4D
RP7- RP20- RP19- RP42- RP40-
RP24 56Ω
RP54-
12C-13 (SH 1) 100 MHZ CLK
12C-5 (SH 1) 2MT CLK
3E 3F 3G 3H 5E 5F 5G 5H 4H 4J 5J
WEB15 WEB14 WEB13 WEB12 WEB11 WEB10 WEB7
WCB15 WCB14 WCB13 WCB12 WCB11 WCB10
WABIS WABIO WAB13 WAB12 WAB11 WAB10
WBB15 WBB14 WBB13 WBB12 WBB11 WBB10
WB2 W2B15 W2B14 W2B13 W2B12 W2B11 W2B10 W2B7
WAB2
WAB6
RP54-2 RP54-3 RP54-4 RP54-5 RP54-6 RP54-7
RP41-2 RP41-9 RP41-10 RP41-5 RP41-6 RP41-7
RP43-3 RP43-9 RP43-10 RP43-5 RP43-6 RP43-7
RP41- RP43-4 RP40-8
R1 120 -2v
R2 120 -2v
R3 120 -2
SAMPLE CLOCK A (+3") P1-42 P1-41
SAMPLE CLOCK B (+2") P1-36 P1-35
SAMPLE CLOCK C (+1") P1-30 P1-29
CONTROL CLK A P1-46 P1-45
CONTROL CLK B P1-40 P1-39
CONTROL CLK C P1-34 P1-33
ASYNCH FORCE ENABLE CONTROL CLK WEB1
SYNCH INHIBIT CONTROL CLK WEB8
INHIBIT CONTROL CLK
CONTROL CLK
CONTROL CLK ENABLE STATUS
P1-28 P1-27 (TO CONTROL BOARD)
MID SOURCED SWING
FORCE BIDIRECTIONALITY WEB2 100-14 (SH 5)
(SH 5) (SW 5) (SW 4)
DO NOT SCALE DRAWING
TOLERANCE
DASH NO NUMBER NEXT ASSEMBLY QTY
ENG SERV DATE
DRAWN Carl Holmes DATE 4-10-81
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
GOULD biomation
TITLE SCHEMATIC CLOCK (WITH LEWEL MEMORY)
SCALE D SIZE PART NUMBER 0114-0161 REV M
CODE K101-D SHEET 3 OF 5


0114-0161
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
J1-19 LEVEL L0
J1-17 LEVEL L1
J1-15 LEVEL L2
J1-13 LEVEL L3
J1-9 ARMED
J1-11
J1-7
J1-3 TRACED
(SH 5) FORCE READ RAMS
J1-5
J1-1 CABLE CONTROL CLOCK
J1-2
J1-20
WCB0 LEVEL MEMORY ADDRESS RESET
5:C/2
11E
11J
11F
12F
12G
12D
12E
11D
10D
11G
12H
10231
10422
10016
10173
10174
RP22-2
RP22-4
RP22-5
RP22-7
RP22-10
RP22-6
RP22-9
RP22-3
RP56-6
RP56-2
RP56-5
RP56-3
RP56-4
RP28-5
RP28-7
RP28-8
RP28-6
RP38-6
RP38-4
RP38-5
RP38-7
RP28-3
RP28-4
RP28-2
RP38-10
RP16-8
RP38-8
RP16-9
RP29-2
RP38-3
RP16-7
RP16-5
RP16-2
RP10-7
RP29-8
RP29-7
RP29-5
RP29-6
RP38-9
RP29-3
RP29-4
RP29-10
RP29-9
ML0
ML1
ML2
ML3
TO 10G (10173) (SH 5)
3½" ≈ 0.5 ms OR MORE
2" ≈ 0.3 ms OR MORE (LAST ON TRACE)
SELECT
R37 120
R36 100
R5 30
R6 680
C1 68 pf
R32 2K
R33 3K
-2V
-5.2V
≈10ns HIGH PULSE WIDTH WHEN "FORCE READ RAMS" BIT IS LOW.
NOTE: WHEN READING RAMS WITH "FORCE READ RAMS" HIGH, TWO CLOCKS ARE REQUIRED FOR EACH READ.
I = C dV/dt
6×10⁻³ = (X×10⁻¹²)·(½)÷(3×10⁻⁹)
X(pf) = 6×10⁻³ × 10¹² × 6×10⁻⁹ × 2
X(pf) = 72 {for 6 ns} ⇒ USE 68pF
GOULD biomation
TITLE SCHEMATIC CLOCK (WITH LEVEL MEMORY)
SCALE D PART NUMBER 0114-0161 REV M
CODE K101-D SHEET 4 OF 5



DWG NO. 0114-0161
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
DIAG LATCH CLK (WB1)
LATCH CLK IS LOW MOST OF THE TIME, TO PASS INFORMATION TRANSPARENTLY
DIAG INTERNAL CLK (WB0B)
FORCE DIAGNOSTIC
CONTROL CLK EN STATUS
MID-SOURCED
MY ADDRESS
FORCE READ RAMS (SH 4)
GOULD biomation
SCHEMATIC CLOCK
WITH LEVEL MEMORY
0114-0161
CODE K101-D
SHEET 5 OF 5



JUMPER LIST						DESCRIPTION	REF DES	AS ETCH	-10	-20	-30	DESCRIPTION	REF DES	AS ETCH	-10	-20	-30
DESCRIPTION	REF DES	AS ETCH	K500 -10	K101 -20	K205 -30	SELECT M/IØ	E13-E14	IN	CUT				E25-E26	IN	CUT		
RS449 RC	E1-E2	IN				SELECT IØ PAGE	E14-E15	OUT	JUMPER				E26-E27	OUT	JUMPER		
INTR 3	E3-E4	IN				RS449 SG	E16-E17	OUT		JMP			E28-E29	OUT		JUMPER	
SELECT A11	E5-E6	IN				RS449 SC	E18-E19	IN	CUT				E30-E31	OUT		JUMPER	
SELECT A10	E7-E8	OUT				SELECT +11V MONITOR	E20-E21	OUT	JUMPER			INTA	E32-E33	IN	CUT		
SELECT A9	E9-E10	OUT				SELECT VBB MONITOR	E21-E22	IN	CUT				E17-E34	IN	CUT	CUT	
SELECT A8	E11-E12	IN											E2-E35	IN	CUT	CUT	
INTR 2	E23-E24	IN															

-50	-40	-30	20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES ± .XX ± .020 .XXX ± .010 HOLE SIZE .X 1 .999 ± .003 .XX 1 .000 .999 ± .004 .XXX 1 .000 .999 ± .005

ENG SERV | DATE

DRAWN: C. WELDON | DATE: 4-30-8

CHECKED

PROJ ENG

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE: ASSEMBLY THRESHOLD/GPIB/RS232

SCALE: 2:1 | SIZE: D | PART NUMBER: 0114-0170 | REV: AB1

CODE K101/K500/K205 | SHEET 1 OF 1

COMMENTS		TOTAL COST	UNIT COST
[1] USED ON K500 ONLY (-10)			
[2] USED ON K101 ONLY (-20)			
[3] USED ON K205 ONLY (-30)			

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1				1	1	1	0114-0172	P.C.B.				
2												
3				2	2	2	7000-0120	EJECTOR				
4				—	—	1	1700-0090	VOLT REG	Q1		LM 317 K	
5				4	4	5	1700-0086	OP AMP	1E, 2E, 5A, 10A / 3E [3]		LM 324A	
6				1	1	1	1700-0063-20	I.C.	3B		REF-01EJ	
7												
8				2	2	2	1820-0077		4A, 9A		AD 7533 LN	
9				11	9	13	1820-0076		1A-1D, 2A, 2D, 5F, 6F, 7F / 2B, 2C, 3A, 3D [3] 2B, 2C [2]		AD 7508	
10				1	1	1	1820-0075		8A		AD 7541	
11				2	2	~	1800-0343		12D / 12E		8251	
12				1	1	1	1800-0344		8E		8253	
13				2	2	~	1700-0101		13A / 13B		1488	
14				2	2	~	1700-0102		14A / 15B		26 LS 32	
15				1	1	—	1800-0200		14B		7433	
16				1	1	1	1800-0125		8D		74 LS 161	
17				13	13	14	1800-0231	I.C.	4B, 5B, 8B, 9B, 4D, 6D, 15D, 5E, 6E, 18E, 19E, 15F, 12B / 5D [1]		74 LS 273	
18												

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	REL PER ERN #0092	12 22 80	SR	[illegible]	
B	REVISED PER ECO #1485			[illegible]	
B	PROD REL ERN #129	3 9 81	MS	[illegible]	
C	REVISED PER ECO # 1579	4 20 81	JWC	JL	
D	REVISED PER ECO # 1700	5 28 81	JWC	JL	
E	REVISED PER ECO #1701	5 28 81	JWC	JL	
F	REVISED PER ECO # 1833	9 21 81	MS	[illegible]	

DASH NO.	NUMBER	QTY
-30	0114-0170-10/-30	1
-20	0114-0002	1
-10	0950-0002	1
NEXT ASSEMBLY		

DRAWN	DATE
SKIDELL	12 22 80
CHECKED [illegible]	4/10/81
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSY
THRESHOLD/GPIB/RS 232

biomation

B | 0114-0170 | REV A,B

MODEL K101 / K500 K205 | CODE | SHEET 1 OF 5

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19				5	5	6	1800-0267	I.C.	13F, 16F, 20F, 16B, 17B, 19F [3]		74 LS 240	
20				5	5	5	1800-0240		8F, 10F, 11F, 16D, 17D		74 LS 244	
21				2	2	2	1800-0268		12F, 14F		74 LS 245	
22				5	5	5	1800-0193		10B, 11B, 9D-11D		74 LS 138	
23				—	—	1	1800-0254		9F		74 LS 85	
24				7	7	7	1800-0311		17F, 18F, 21F, 18D, 19D, 20E, 21E		7438	
25				1	1	1	1800-0110		18B		74 LS 10	
26				3	3	3	1800-0105		21D, 19B, 20D		74 LS 00	
27				4	4	4	1800-0068		20A, 21A, 20B, 21B		74 LS 112	
28				1	1	1	1800-0111		12A		74 LS 20	
29				1	1	1	1800-0309	I.C.	19A		74 LS 260	
30												
31				1	1	1	1700-0071	I.C.	7E		LF356 AN	
32				1	1	1	1700-0106	I.C.	7A		OP-11E	
33				3	3	3	3000-3300	RESISTOR	R15 R23, 33		330, 1/4W 5%	
34				6	6	4	-2201		R20, 24, 28, 30, R14, 19 [2] [3]		2.2K,	
35				4	4	4	-1001		R35-38		1K,	
36				3	3	3	3000-2200	RESISTOR	R16, 22, 32		220, 1/4W 5%	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
G	REVISED PER ECO #1885	9 21 81	MS	[illegible]	
H	REVISED PER ECO #1867	9 21 81	MS	[illegible]	
J	REVISED PER ECO #1805	9 22 81	BH	[illegible]	
K	REVISED PER ECO #1954	9-22 81	BH	[illegible]	
L	REVISED PER ECO # 2179	11		[illegible]	
M	REVISED PER ECO # 2202	1-19-82	JWC	[illegible]	
N	REVISED PER ECO # 2240	1-19-82	JWC	[illegible]	

DASH NO.	NUMBER	QTY
NEXT ASSEMBLY		

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSY
THRESHOLD/GPIB/RS 232

biomation

B | 0114-0170 | REV A,B

MODEL K101 / K500 K205 | CODE | SHEET 2 OF 5

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37				2	2	–	3000-1004	RESISTOR	R40, 41		1M, ¼W, 5%	
38				1	1	1	3090-2006		R31		20, ¼W, 5%	
39				1	1	1	3000-5106		R34		51, ¼W, 5%	
40				1	1	1	3000-2701		R21		2.7K, ¼W, 5%	
41				3	3	1	3000-2002		R19 R42,43 [2][5]		20K, ¼W, 5%	
42				–	–	2	3000-3600		R10, 12		360, ¼W, 5%	
43				–	~	1	3100-1240		R25		124, ⅛W, 1%	
44				–	~	1	3100-9760		R26		976,	
45				1	1	3	3100-1003		R4 R11,13 [1]		100K,	
46				1	1	1	3100-4990		R17		499, ⅛W, 1%	
47				2	2	~	3000-3302	RESISTOR	R11,13		33K, ¼W, 5%	
48				3	3	3	3300-0070	POT	R7,8,44		10K, 20T	
49				4	4	6	3300-0060	POT	R2,3,5,9 R1,6 [1]		500, 20T	
50				2	2	–	3300-0012	POT	R1,6		1KΩ, 20T	
51				4	4	3	3700-0048	RES PACK	6A,11A,4E 7 TO [2][5]		10K, .1%, 16 PIN	DIP
52				2	2	3	3700-0083		RP10,11 RP22 [1]		2.2K 10 PIN	SIP
53				9	9	9	3700-0049		RP12-18, 20, 23		3K/6.2K 10 PIN	SIP
54				2	1	~	3700-0084	RES PACK	RP2 [2][5] RP6 [3]		2.7K, 8 PIN 4 RES	SIP

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
P	REVISED PER ECO #2242	1-29-82	DM	MW	
Q	REVISED PER ECO # 2498	4-19-82	MW	RW	
R	REVISED PER ECO # 2501	4-19-82	MW	RW	
S	REVISE PER ECO # 2644	5-28-82	MW	T.J.	
T	REVISED PER ECO # 2703	11-9-82	MW	DMW 12/6/82	
U	REVISED PER ECO # 3589	3/14/83	MW	DMW	3-16-83
V	REVISED PER ECO # 3605	3/15/83	MW	DMW	3-16-83

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSY
THRESHOLD / GPIB / RS 232

biomation

B | 0114-0170 | REV A&B

DASH NO. | NUMBER | QTY
NEXT ASSEMBLY

MODEL K101/K500 K205 | CODE | SHEET 3 OF 5

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	20	10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55				4	5	2	3700-0056	RES PACK	RP19, 21 RP1,5 [1] RP1,5,6 [2]		180, 8 PIN	SIP
56				2	2	3	3700-0076	RES PACK	RP7, 8 RP9 [1]		47, 8 PIN	SIP
57				2	2	–	3000-7500	RESISTOR	R10, 12		750, 1/4W, 5%	
58				2	2	2	1000-0003	DIODE	CR1,2		HP 5082-2811	
59				1	1	1	1300-0028	TRANSISTOR	Q2		2N3904	
60				1	1	1	1400-0019	TRANSISTOR	Q3		2N3906	
61				1	1	1	3000-2001	RESISTOR	R27		2K, 1/4W 5%	
62				1	1	1	3000-3001	RESISTOR	R29		3K, 1/4W 5%	
63				46	46	47	4010-0103	CAP, CERAMIC	C1 2 b, 7,9,11,14-32, 34-37, 39-41, 43-51, 60,61,75,78,79 [1] C42		.01 μf	
65				14	14	14	4010-0470	CAP, CERAMIC	C3-5, 7,10,13, 33, 38, 53-57, 59		47 pf	
66				1	1	1	4010-0471	CAP, CERAMIC	C77		470pf, 100V, 5%	
67				12	12	12	4010-0104	CAP, CERAMIC	C 63-72, 52, 58		.1 μf	
68				2	2	3	4400-0045	CAP,	C73, 74 C62 [1]		33 μf, 25 V ALUM.	
69				1	1	1	4400-0043	CAPACITOR	C 76		47 μf, 6V ALUM.	
70												
71				1	1	1	6000-0417	HEADER	P4		6 PIN	
72				1	1	1	6000-0388-20	HEADER	P3		26 PIN, SHORT EARS	

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
W	REVISED PER ECO # 3706	5/6/83	MW	DMW	5/6/83
X	REVISED PER ECO # 4068	4/18/84	DMW	DMW	4/18/84
Y	REVISED PER ECO # 4111	1/11/84	JC	DCN	1/27/84
Z	REVISED PER ECO # 4087	1/23/84	JC	DCN 2/28/84	AR
AA	REVISED PER ECO # 4277	2/6/84	JC	DCN 2/28/84	2/28/84
AB	REVISED PER ECO # 4384	2-28-84	JC	DCN 3/14/84	3/14/84

DRAWN	DATE
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL
ASSY
THRESHOLD / GPIB / RS 232

biomation

B | 0114-0170 | REV A&B

DASH NO | NUMBER | QTY
NEXT ASSEMBLY

MODEL K101/K500 K205 | CODE | SHEET 4 OF 5

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	20	10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
73				—	-	1	7000-0418	HEAT SINK	@ Q1			
74				2	2	1	6100-0119	SOCKET 14 PIN DIP	X7A X4B			
75				2	2	2	6100-0120	SOCKET 16 PIN DIP	X 4A, 9A			
76				1	1	1	6100-0049	SOCKET 18 PIN DIP	X 8A			
77				1	1	1	6100-0122	SOCKET 24 PIN DIP	X 8E			
78				2	2	~	6100-0151	SOCKET 28 PIN DIP	X 12D, X12E			
79												
80				—	—	1	7200-0016	INSULATOR			TO-3	
81				—	—	2	7000-0221	WASHER			#4 INSULATING	
82				—	—	2	———	SCREW			#4-40 P.H.	
83				—	—	2	———	WASHER			#4 FLAT	
84				—	—	2	———	KEP NUT			#4-40	
85												
86				8	8	8	9000-0054	BUS WIRE			GND STRAP	
87												
88												
89												
90												

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

	DATE
DRAWN	
CHECKED	
ENGINEER	
MANUFACTURING	
QUALITY ASSURANCE	

LIST OF MATERIAL

ASSY

THRESHOLD / GPIB / RS 232

MODEL K101 / K205 K500

biomation

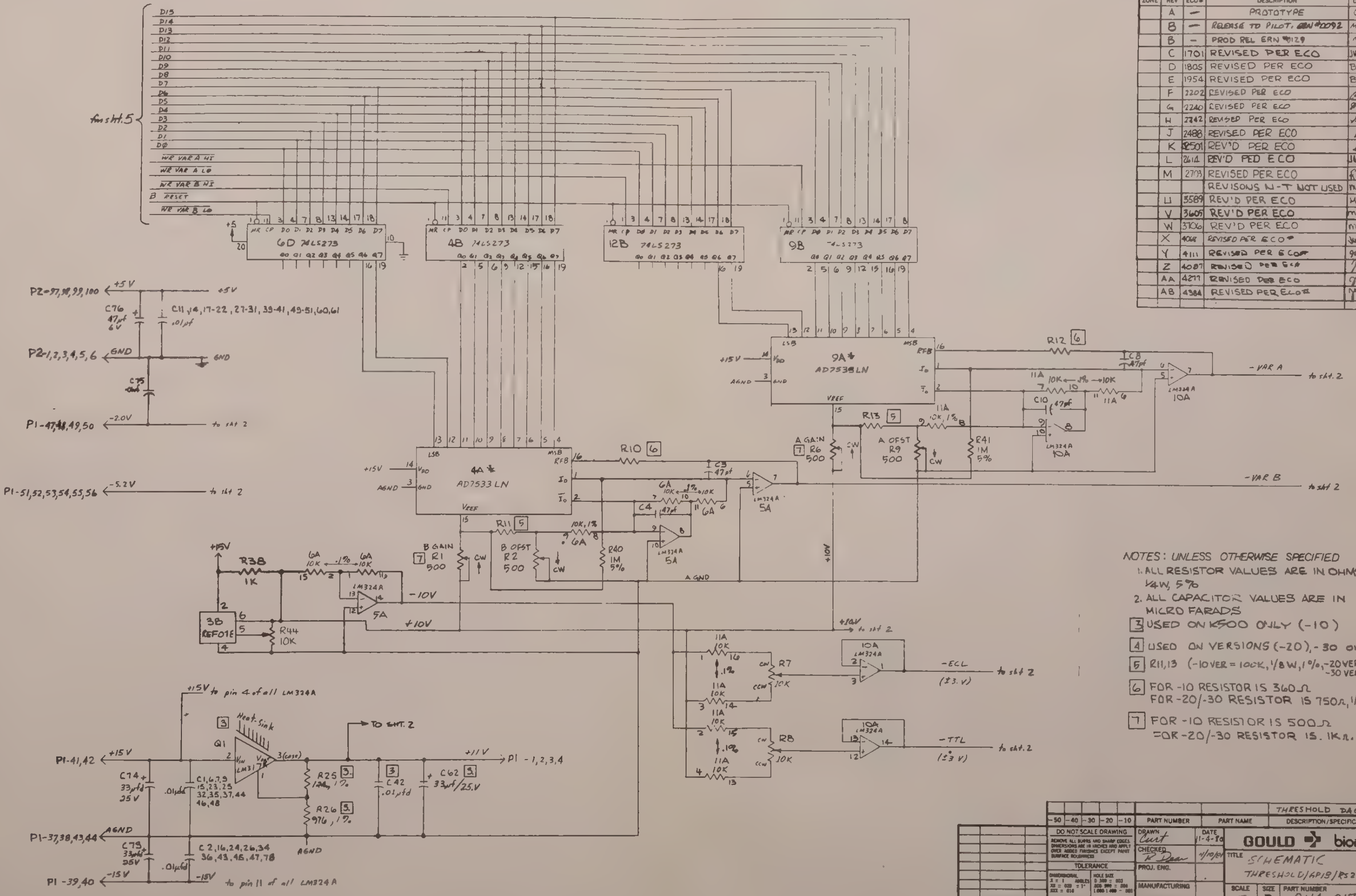
B 0114-0170 REV A5

CODE

SHEET 5 OF 5

DWG NO 0114-0171 SH 1 REV AB

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—	PROTOTYPE	CB		
	B	—	RELEASE TO PILOT, ERN #0092	MR		
	B	—	PROD REL ERN #0129	MB		4/81
	C	1701	REVISED PER ECO	JWC	JL	
	D	1805	REVISED PER ECO	BH	JW	
	E	1954	REVISED PER ECO	B H.	JW	7/81
	F	2202	REVISED PER ECO		JW	
	G	2240	REVISED PER ECO		JW	
	H	2242	REVISED PER ECO		JW	
	J	2488	REVISED PER ECO			
	K	2501	REV'D PER ECO			
	L	2614	REV'D PER ECO	JWC	T.J.	
	M	2703	REVISED PER ECO		JW	
			REVISONS N-T NOT USED	MW	DLW	
	U	3589	REV'D PER ECO	MW	DLW	3-86
	V	3605	REV'D PER ECO	MW	DLW	3-86
	W	3706	REV'D PER ECO	MW	DLW	
	X	4068	REVISED PER ECO			
	Y	4111	REVISED PER ECO			
	Z	4087	REVISED PER ECO			
	AA	4277	REVISED PER ECO			
	AB	4384	REVISED PER ECO			



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS

[3] USED ON K500 ONLY (-10)

[4] USED ON VERSIONS (-20), -30 ONLY

[5] R11,13 (-10 VER = 10K, 1/8W, 1%, -20 VER = 33K, -30 VER = 33K

[6] FOR -10 RESISTOR IS 360Ω FOR -20/-30 RESISTOR IS 750Ω, 1/8W, 1%

[7] FOR -10 RESISTOR IS 500Ω FOR -20/-30 RESISTOR IS 1KΩ.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
							THRESHOLD DAC'S	1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DASH NO | NUMBER NEXT ASSEMBLY | QTY

ENG. SERV | DATE

DRAWN Curt DATE 11-4-80

CHECKED R Dean 4/10/81

PROJ. ENG.

MANUFACTURING

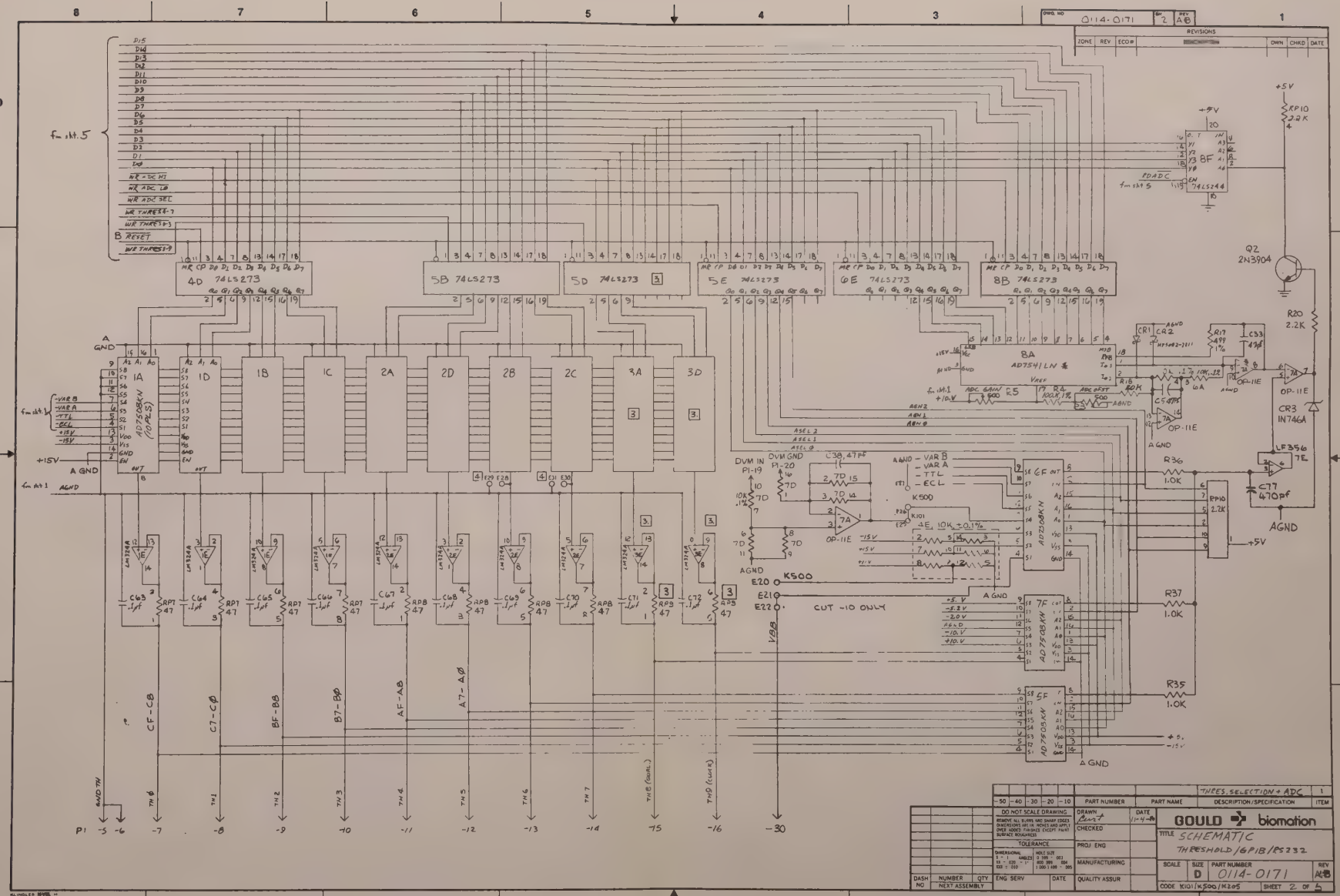
QUALITY ASSUR

GOULD biomation

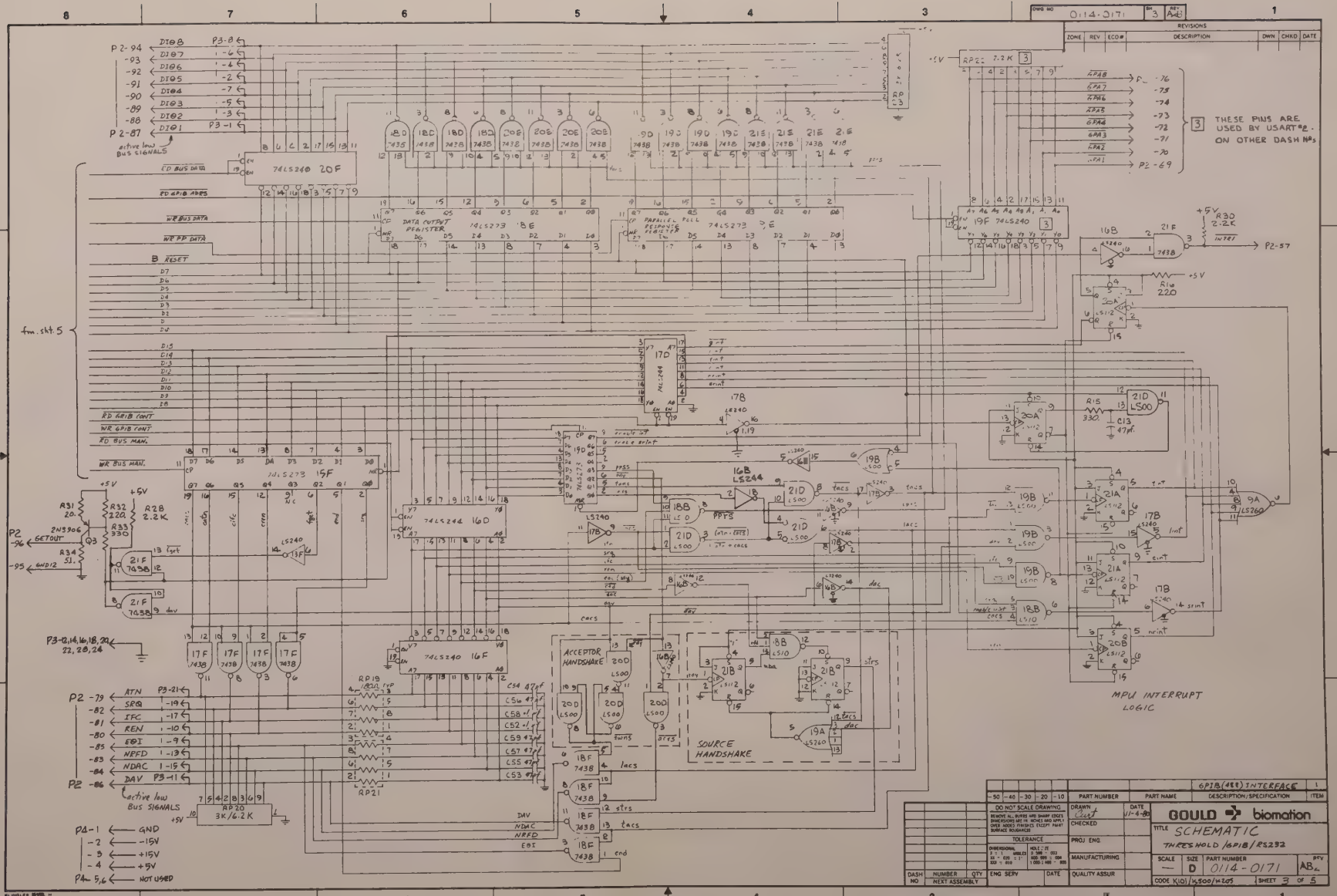
TITLE SCHEMATIC THRESHOLD/GPIB/RS232

SCALE — SIZE D PART NUMBER 0114-0171 REV AB

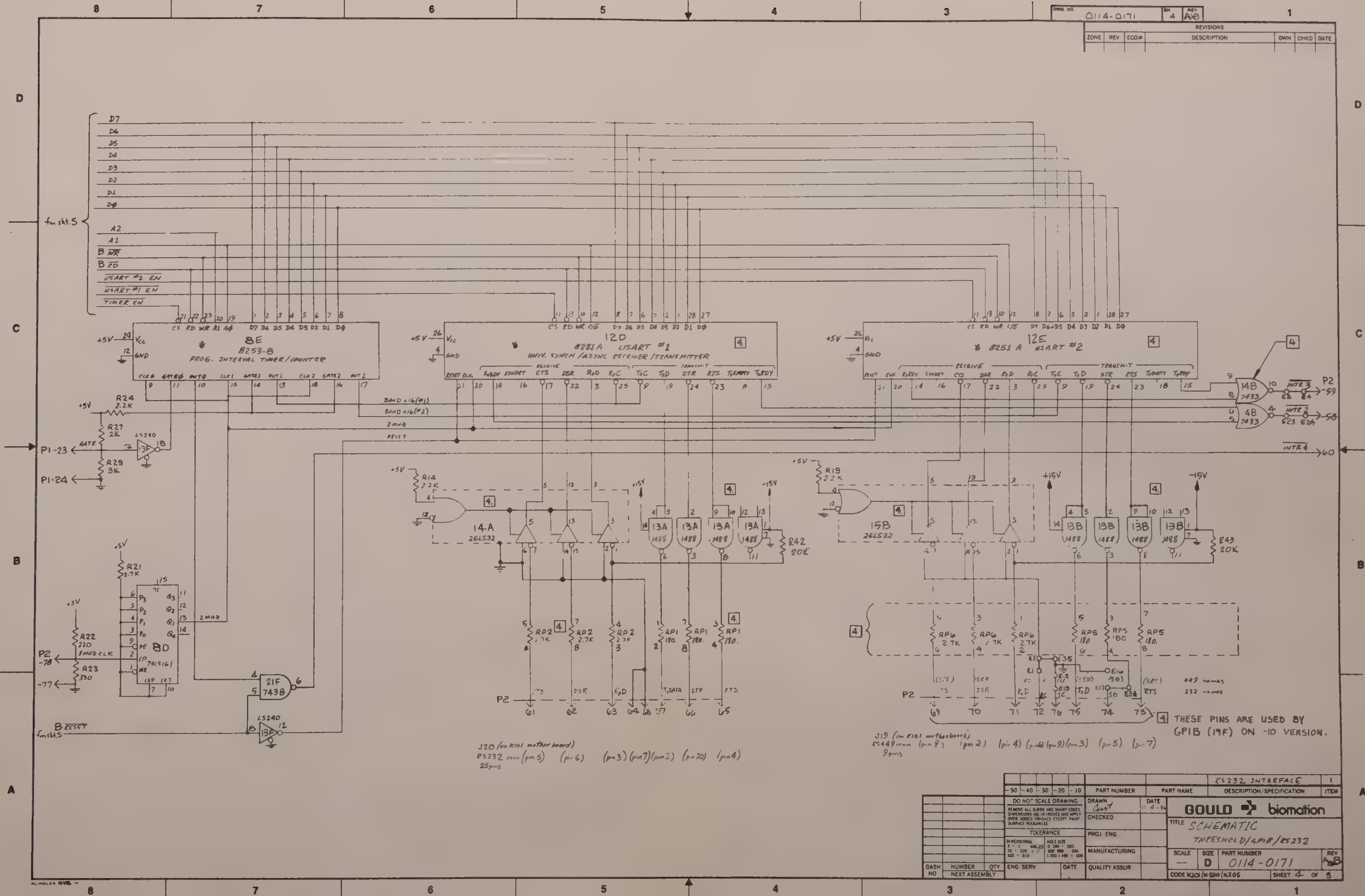
CODE K101/K500/K205 SHEET 1 OF 3

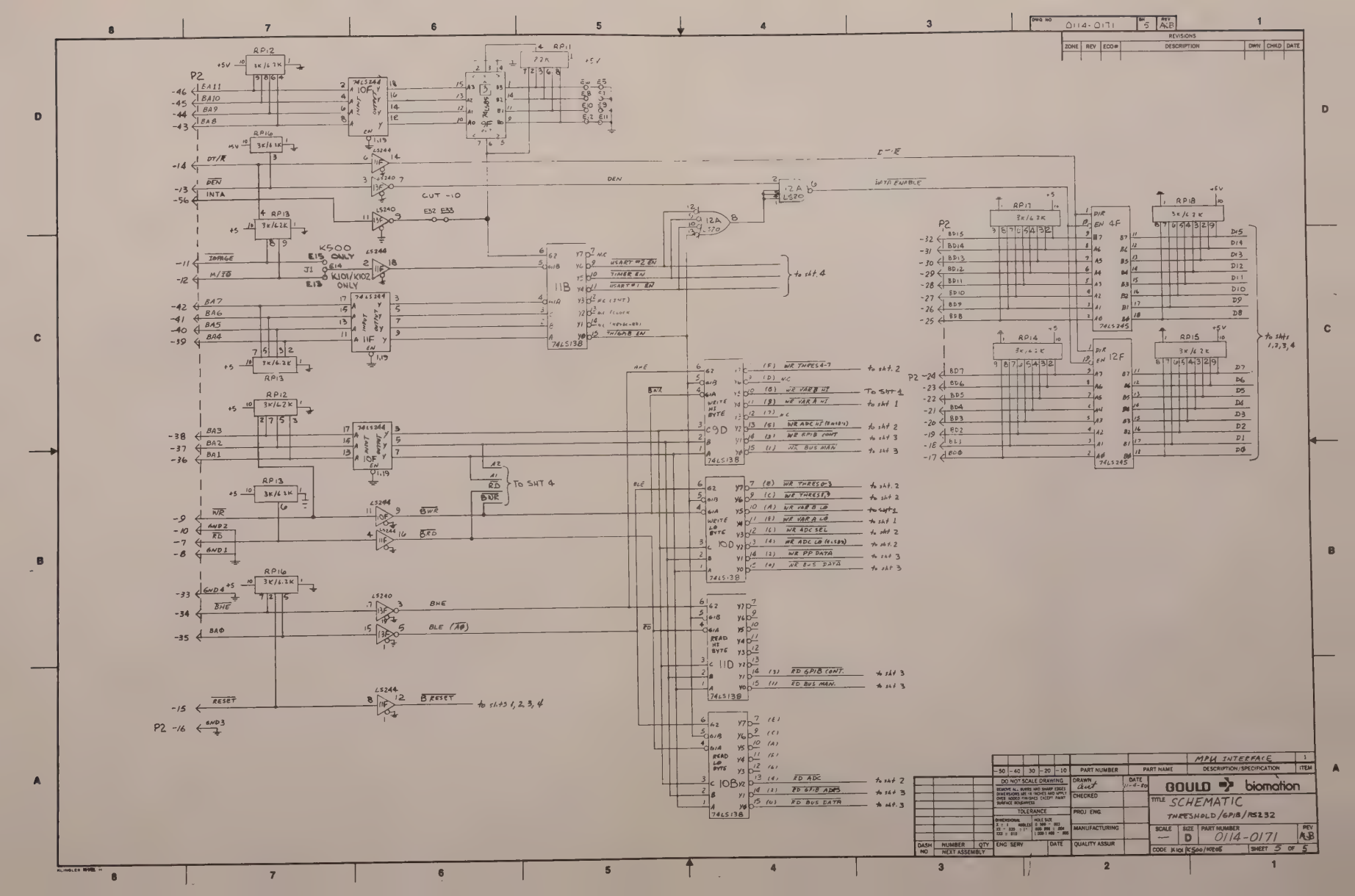


DWG. NO 0114-0171
SH 2
REV A&B
REVISIONS
ZONE
REV
ECO#
DWN
CHKD
DATE
4D 74LS273
5B 74LS273
5D 74LS273
5E 74LS273
6E 74LS273
8B 74LS273
8A AD7541LN
1A
1D
1B
1C
2A
2D
2B
2C
3A
3D
AD7508KN (10PLS)
AD7508KN
6F
7F
5F
8F 74LS244
Q2 2N3904
CR3 1N746A
LF356 7E
OP-11E
RP10 2.2K
R20 2.2K
R36 1.0K
R37 1.0K
R35 1.0K
C77 470pf
AGND
+5V
-15V
+15V
A GND
DVM IN PI-19
DVM GND PI-20
C38, 47pf
K500
K101
CUT -10 ONLY
VBB
CF-CB
C7-CØ
BF-BB
B7-BØ
AF-AB
A7-AØ
GND TH
TH Ø
TH 1
TH 2
TH 3
TH 4
TH 5
TH 6
TH 7
TH 8 (DUAL)
TH 9 (CLOCK)
P1
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
-15
-16
-30
THRES. SELECTION + ADC
1
-50
-40
-30
-20
-10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL
HOLE SIZE
DRAWN
DATE 11-4-80
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
GOULD biomation
TITLE SCHEMATIC
THRESHOLD/GPIB/RS232
SCALE
SIZE D
PART NUMBER 0114-0171
REV A&B
CODE K101/K500/K205
SHEET 2 OF 5
DASH NO
NUMBER
QTY
NEXT ASSEMBLY

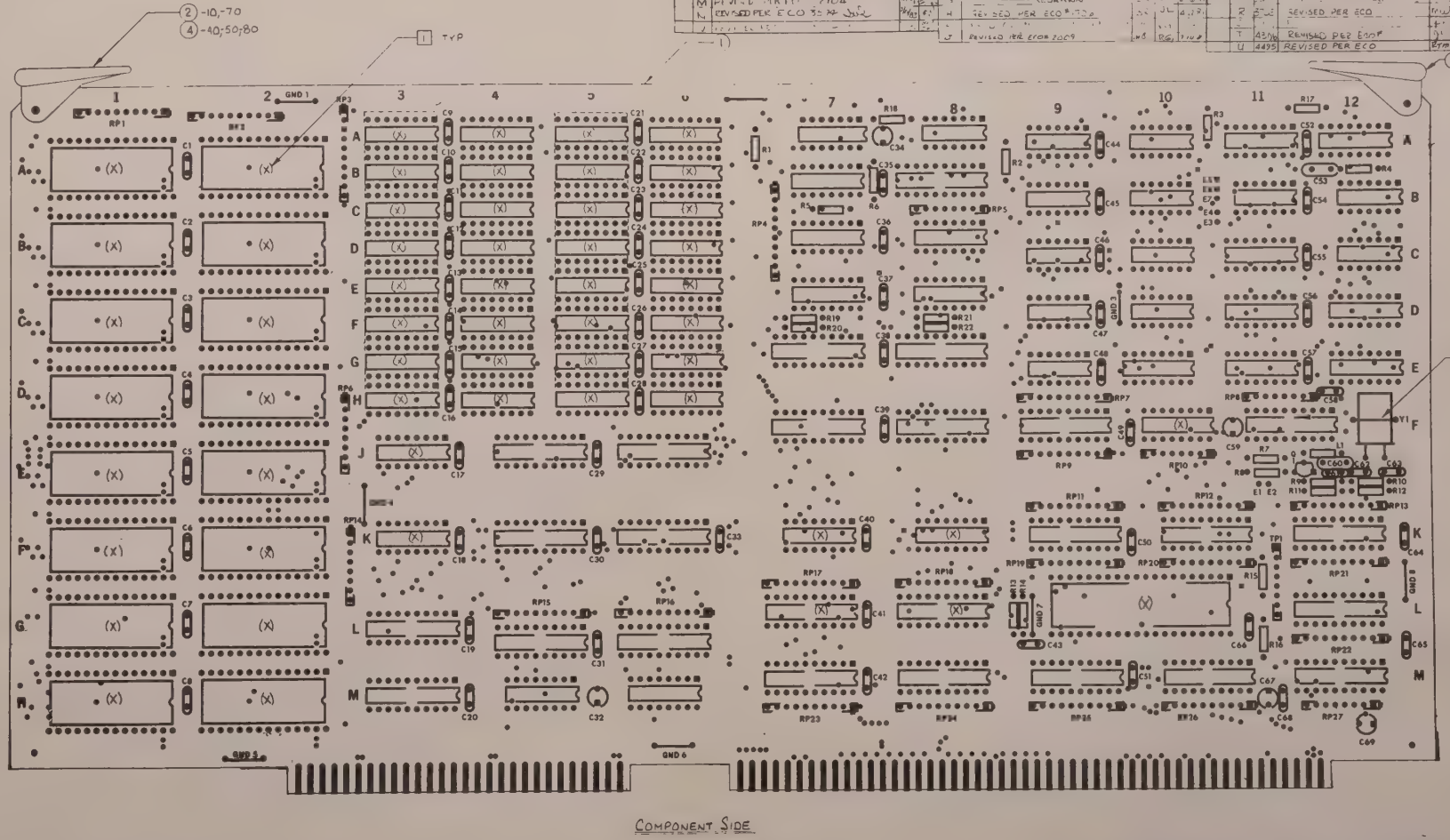


DWG NO 0114-0171
SH 3
REV AB
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
THESE PINS ARE USED BY USART #2 ON OTHER DASH NOs
MPU INTERRUPT LOGIC
ACCEPTOR HANDSHAKE
SOURCE HANDSHAKE
DATA OUTPUT REGISTER
PARALLEL POLL RESPONSE REGISTER
74LS240 20F
74LS273 18E
74LS273 9E
74LS273 15F
74LS244 16D
74LS240 16F
RP20 3K/6.2K
RP22 2.2K
RP19 180Ω TYP
RP21
fm. sht. 5
active low BUS SIGNALS
P2-94 DIO8 P3-8
-93 DIO7 -6
-92 DIO6 -4
-91 DIO5 -2
-90 DIO4 -7
-89 DIO3 -5
-88 DIO2 -3
P2-87 DIO1 P3-1
RD BUS DATA
RD GPIB ADRS
WR BUS DATA
WR PP DATA
B RESET
RD GPIB CONT
WR GPIB CONT
RD BUS MAN.
WR BUS MAN.
P3-12,14,16,18,20 22,28,24
P2-79 ATN P3-21
-82 SRQ -19
-81 IFC -17
-80 REN -10
-85 EOI -9
-83 NRFD -13
-84 NDAC -15
P2-86 DAV P3-11
P4-1 GND
-2 -15V
-3 +15V
-4 +5V
P4-5,6 NOT USED
GPIB(488) INTERFACE
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DO NOT SCALE DRAWING
DRAWN Curt DATE 11-4-80
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV DATE
DASH NO NUMBER QTY NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC
THRESHOLD/GPIB/RS232
SCALE — SIZE D PART NUMBER 0114-0171 REV AB
CODE K101/K500/K205 SHEET 3 OF 5


DWG NO 0114-0171 SH 4 REV A/B
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
fm sht.5
D7 D6 D5 D4 D3 D2 D1 DØ
A2 A1 B WR B RD
USART #2 EN
USART #1 EN
TIMER EN
8E 8253-B PROG. INTERVAL TIMER/COUNTER
12D 8251A USART #1 UNIV. SYNCH/ASYNC RECEIVER/TRANSMITTER
12E 8251A USART #2
BAUD x16(#1)
BAUD x16(#2)
2MHZ
RESET
INTR 3
INTR 2
INTR 4
P1-23
P1-24
GATE
R24 2.2K
R27 2K
R29 3K
LS240
14A 26LS32
15B 26LS32
13A 1488
13B 1488
R42 20K
R43 20K
R14 2.2K
R19 2.2K
R21 2.7K
R22 220
R23 330
8MHZ CLK
8D 74LS161
2MHZ
21F 7438
B RESET fm sht.5
RP2 2.7K
RP1 180
RP6 2.7K
RP5 180
P2
449 names
232 names
THESE PINS ARE USED BY GPIB (19F) ON -10 VERSION.
J20 (on K101 mother board) RS232 conn (pin 5) (pin 6) (pin 3) (pin 7) (pin 2) (pin 20) (pin 4) 25 pins
J19 (on K101 motherboard) RS449 conn (pin 8) (pin 2) (pin 4) (pin 9) (pin 3) (pin 5) (pin 7) 9 pins
RS232 INTERFACE
PART NUMBER PART NAME DESCRIPTION/SPECIFICATION ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN CHECKED PROJ ENG MANUFACTURING QUALITY ASSUR
GOULD biomation
TITLE SCHEMATIC THRESHOLD/GPIB/RS232
SCALE — SIZE D PART NUMBER 0114-0171 REV A/B
CODE K101/K500/K205 SHEET 4 OF 5
DASH NO NUMBER QTY NEXT ASSEMBLY ENG SERV DATE



DWG NO 0114-0171
SH 5
REV A&B
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
RP12 3K/6.2K
RP11 22K
RP16 3K/6.2K
RP13 3K/6.2K
RP17 3K/6.2K
RP18 3K/6.2K
RP14 3K/6.2K
RP15 3K/6.2K
74LS244 10F
74LS245 9F
74LS138 11B
74LS138 11F
74LS244 10F
74LS138 9D
74LS138 10D
74LS138 11D
74LS138 10B
74LS245 4F
74LS245 12F
LS240
LS244
LS20
K500 ONLY
K101/K102 ONLY
CUT -10
DATA ENABLE
to sht. 4
to shts 1,2,3,4
To SHT 4
WR THRES 4-7
WR VAR B HI
WR VAR A HI
WR ADC HI
WR GPIB CONT
WR BUS MAN
WR THRES 0-3
WR THRES 8,9
WR VAR B LO
WR VAR A LO
WR ADC SEL
WR ADC LO
WR PP DATA
WR BUS DATA
RD GPIB CONT.
RD BUS MAN.
RD ADC
RD GPIB ADDS
RD BUS DATA
BWR
BRD
BHE
BLE (A0)
B RESET
RESET
GND1
GND2
GND3
GND4
DT/R
DEN
INTA
IOPAGE
M/IO
WR
RD
BA0
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BA10
BA11
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
P2
MPU INTERFACE
DO NOT SCALE DRAWING
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC
THRESHOLD/GPIB/RS232
SCALE —
SIZE D
PART NUMBER 0114-0171
REV A&B
CODE K101 K500/K1005
SHEET 5 OF 5



NOTES:
1. THIS SYMBOL (X) INDICATES WHERE I.C. SOCKETS ARE REQUIRED (FOR REF ONLY)

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	R	3[illegible]	REVISED PER ECO			
	T	43[illegible]	REVISED PER ECO#			
	U	4495	REVISED PER ECO			

DWG NO 0114-0185 SH 1 REV V

DASH NO	NUMBER	QTY
-50	0114-0002	1
-40	0114-0002	1
-30	0114-0003	1
-20	0114-0002	1
-10	0950-0002	1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONS: X = ± .1 ; .XX = ± .020 ; .XXX = ± .010
HOLE SIZE: .000 - .999 ± .004 ; 1.000 - 1.999 ± .005

ENG SERV
DRAWN [illegible] DATE 4-16-84
CHECKED KG 5/29/84
PROJ ENG
MANUFACTURING
QUALITY ASSUR
DATE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

GOULD biomation

TITLE: ASSEMBLY, K101, K500 MPU BD.

SCALE	SIZE	PART NUMBER	REV
2:1	D	0114-0185	V

CODE K101, K500 SHEET 1 OF 1

GOULD

TITLE		DRAWING NO.	REV
ASSEMBLY MPU PWB	LM	0114-0185	V

DWN	CHK	ENG	MFG	MODEL	SHEET
12-2-84	DGW			K101, K102 K500	1 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
1.	0114-0187	1	–			–		MPU P.C. BOARD	
2.	7000-0120	–	2			1		EJECTOR	LEFT SIDE (A11) (& RIGHT ON -10,-70)
3.	0114-0185-05	–	1			1		MPU BOARD SUB ASSEMBLY	
4.	0112-0228-07	–	–			1		EJECTOR, STAMPED A7	RIGHT SIDE (A12)
5.									
6.									
7.	0950-0191	–	1			–		I.C.	10F ROM, ADD. MAP
8.	0950-0193	–	1			–			3J ROM, CHIP SEL
9.	0950-0192	–	1			–			3K ROM. CHIP SEL
10.									
11.	0114-0066	–	–			1			10F ROM ADD. MAP
12.	0114-0067	–	–			1			3J ROM, CHIP SEL
13	0114-0069	–	–			1			3K ROM, CHIP SEL
14.									
15.	1800-0321	–	1			1		IC.	10L 8086
16.	0117-0017-01	–	–			–		I.C, ROM ADD MAP	10F

REV	ECO	CHK	APPD	DATE
T	4306	DGW	JWS	4/4/84
U	4494	DGW	JWS	7/10/84
V	4581	DGW	JWS	9/17/84

NOTES:

DASH #	NEXT ASSY	QTY
-10	0950-0002	1
-20	0114-0002	1
-30	0114-0073	1
-40	0114-0002	1
-50	0114-0002	1

GOULD

TITLE		DRAWING NO.	REV
ASSEMBLY MPU PWB	LM	0114-0185	V

DWN	CHK	ENG	MFG	MODEL	SHEET
12-2-84					2 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-90	U/M	DESCRIPTION	REFERENCE DESIGNATION
1.	0114-0187	–		–	–			P.C. BOARD	
2.	7000-0120	1		2	1			EJECTOR	
3.	0114-0185-05	1		1	1			MPU BOARD SUBASSEMBLY	
4.	0112-0228-07	1		–	1			EJECTOR STAMPED A7	
5									
6.									
7.	0950-0191	–		–	–			I.C.	10F ROM ADD MAP
8.	0950-0193	–		–	–				3J ROM CHIP SEL
9.	0950-0192	–		–	–				3K ROM CHIP SEL
10.									
11.	0114-0066	1		–	1				10F ROM ADD MAP
12.	0114-0067	1		–	1				3J ROM CHIP SEL
13.	0114-0069	1		–	1				3K ROM CHIP SEL
14.									
15	1800-0321	1		1	1			I.C.	10L 8086
16.	0117-0017-01	–		1	–			I.C. ROM ADD MAP	10F

REV	ECO	CHK	APPD	DATE

NOTES: BASIC -05 SUBASSEMBLY
-10: K500 -20: N/A -30 N/A
-40: K101 WITH STORAGE
-50: K102 WITH STORAGE -60: N/A
-70: K105 -80: K205

DASH #	NEXT ASSY	QTY

GOULD

TITLE ASSEMBLY MPU PWB | LM | DRAWING NO. 0114-0185 | REV V

MODEL | SHEET 3 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
17.	0117-0018-01	—	—			—		I.C., ROM CHIP SEL	3J
18.	0117-0019-01	—	—			—		I.C., ROM CHIP SEL	3K
19.									
20.	1800-0359	—	—			32		I.C. 4164, 64K RAM	3A-3H, 5A-5H, 4A-4H, 6A-6H
21.	6100-0120	37	—			—		SOCKET, 16 PIN DIP, LP	X3J, X3K, X7K, X8K, X10F, X3A-X3H, X4A-X4H, X5A-X5H, X6A-X6H
22.									
23.	1400-0019	1	—			—		TRANSISTOR 2N3906	Q1
24.									
25.	1800-0031	3	—			—		I.C. 74S00, 14	9B, 10B, 12B
26.	1800-0038	1	—			—		74S20	9C
27.	1800-0039	8	—			—		74S112	10E, 11A, 11C, 11D, 11E, 12A, 12D, 12E
28.	1800-0060	4	—			—		74S10	7A, 8A, 9D, 12C
29.	1800-0092	1	—			—		74S04	10A
30.	1800-0107	1	—			—		74LS04	9E
31.	1800-0125	4	—			—		74LS161	7C, 7D, 8C, 8D
32.	1800-0133	1	—			—		74S11	10C
33.	1800-0136	1	—			—		74S51	10D
34.	1800-0208	1	—			—		74S161	7B
35.	1800-0240	9	—			—		74LS244	3L, 3M, 4J, 6J, 7E, 7F, 8E, 8F, 9F
36.	1800-0243	2	—			—		I.C. 74S08	9A, 11B

GOULD

TITLE ASSEMBLY MPU PWB. | LM | DRAWING NO. 0114-0185 | REV V

MODEL | SHEET 4 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	U/M	DESCRIPTION	REFERENCE DESIGNATION
17.	0117-0018-01	—		1	—		I.C. ROM CHIP SEL	
18.	0117-0019-01	—		1	—		I.C. ROM CHIP SEL	
19.								
20.	1800-0353	32		32	32		I.C. 4164, 64K RAM	
21.	6100-0120	—		—	—		SOCKET, 16PIN DIP, LP	
22.								
23.	1400-0019	—		—	—		TRANSISTOR, 2N3906	
24.								
25.	1800-0031	—		—	—		I.C. 74S00	
26.	1800-0038	—		—	—		74S20	
27.	1800-0039	—		—	—		74S112	
28.	1800-0060	—		—	—		74S10	
29.	1800-0092	—		—	—		74S04	
30.	1800-0107	—		—	—		74LS04	
31.	1800-0125	—		—	—		74LS161	
32.	1800-0133	—		—	—		74S11	
33.	1800-0136	—		—	—		74S51	
34.	1800-0208	—		—	—		74S161	
35.	1800-0240	—		—	—		74LS244	
36.	1800-0243	—		—	—		I.C. 74S08	

GOULD

TITLE ASSEMBLY MPU PWB | LM | DRAWING NO. 0114-0185 | REV V

MODEL | SHEET 5 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
37.	1800-0268	2	–			–		I.C. 74LS245	7M, 8M
38.	1800-0298	10	–			–		I.C. 74LS373	4K,4L,6K,6L,9K,9M,10K,10M,11K,11L
39.	1800-0320	–	16			–		I.C. 2118 RAM	4A-4H, 6A-6H
40.	1800-0335	2	–			–		I.C. 74LS166	4M, 6M
41.	1800-0353	–	–			–		I.C.	4A-4H, 6A-H
42.	1800-0261	3	–			–		I.C. 74S240	8B, 11F, 11M
43.	2100-0009	1	–			–		INDUCTOR 1.5uH	L1
44.									
45.									
46.	3000-1000	1	–			–		RESISTOR, 100Ω, 1/4 W, 5%	R11
47.	3000-1300	1	–			–		130Ω	R9
48.	3000-1601	2	–			–		1.6K	R6, 10
49.	3000-2006	1	–			–		20Ω	R4
50.	3000-2200	3	–			–		220	R7, 19, 21
51.	3000-2201	7	–			–		2.2K	R1-3, 5, 15, 17, 18
52.	3000-2700	1	–			–		270Ω	R13
53.	3000-3300	3	–			–		330Ω	R8, 20, 22
54.	3000-3301	1	–			–		3.3K	R12
55.	3000-5100	1	–			–		510Ω	R16
56.	3000-9106	1	–			–		91Ω 1/4W 5%	R14

GOULD

TITLE ASSEMBLY MPU PWB | LM | DRAWING NO. 0114-0185 | REV V

MODEL | SHEET 6 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-	U/M	DESCRIPTION	REFERENCE DESIGNATION
37.	1800-0268	–		–	–			I.C. 74LS245	
38.	1800-0298	–		–	–			I.C. 74LS373	
39.	1800-0320	–		–	–			I.C. 2118 RAM	
40.	1800-0335	–		–	–			I.C. 74LS166	
41.	1800-0353	–		–	–			I.C.	
42.	1800-0261	–		–	–			I.C. 74S240	
43.	2100-1000	–		–	–			INDUCTOR 1.5uH	
44.									
45.									
46.	3000-1000	–		–	–			RESISTOR 100Ω, 1/4W, 5%	
47.	3000-1300	–		–	–			130Ω	
48.	3000-1601	–		–	–			1.6K	
49.	3000-2006	–		–	–			20Ω	
50.	3000-2200	–		–	–			220Ω	
51.	3000-2201	-		–	–			2.2K	
52.	3000-2700	–		–	–			270Ω	
53.	3000-3300	–		–	–			330Ω	
54.	3000-3301	–		–	–			3.3K	
55.	3000-5100	–		–	–			510Ω	
56.	3000-9106	–		–	–			RESISTOR 91Ω	

GOULD

TITLE		DRAWING NO.	REV
ASSEMBLY MPU PWB	LM	0114-0185	V
	MODEL	SHEET 7 OF 12	

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
57.	3700-0049	13	–			–		RES. PAK, 3K/6.2K, 10 PIN SIP	RP1,2,7,9,15-18,22-26
58.	3700-0057	6	–			–		RES. PAK, 2.2K, 8 PIN SIP	RP5,6,8,10,14,27
59.	3700-0065	5	–			–		RES. PAK, 220/330, 10 PIN SIP	RP3,4,11-13
60.	3700-0066	3	–			–		RES. PAK, 10K, 10 PIN SIP	RP19-21
61.									
62.									
63.	4000-0040	1	–			–		CAP. 470pf	C43
64.	4000-0044	61	–			1		CAP. .01uf, ±20%, 100V	C1-31,33,35-42,54-58,61-66,
65.									68,44-52 (67 -20,30,48,50)
66.									
67.	4100-0019	1	–			–		CAP. 50pf	C53
68.	4100-0029	1	–			–		CAP. 30pf	C60
69.									
70.	4400-0043	4	1			–		CAP. 47uf, ±10%, 6V	C32,34,59,69 (67 -10,-70,-80)
71.									
72.	5100-0016	1	–			–		CRYSTAL, 24MHZ	Y1
73.									
74.	6000-0190	1	–			–		HEADER, 8 PIN CONN	TP1
75.									
76.									

GOULD

TITLE		DRAWING NO.	REV
ASSEMBLY MPU PWB	LM	0114-0185	V
	MODEL	SHEET 8 OF 12	

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-90	U/M	DESCRIPTION	REFERENCE DESIGNATION
57.	3700-0049	–		–	–			RES. PAK, 3K/6.2K, 10 PIN SIP	
58.	3700-0057	–		–	–			RES. PAK, 2.2K, 8 PIN SIP	
59.	3700-0065	–		–	–			RES. PAK, 220/330, 10 PIN SIP	
60.	3700-0066	–		–	–			RES. PAK, 10K, 10 PIN SIP	
61.									
62.									
63.	4000-0040	–		–	–			CAP. 470pf	
64.	4000-0044	1		–	–			CAP. .01uf, ±20%, 100V	
65.									
66.									
67.	4100-0019	–		–	–			CAP. 50pf	
68.	4100-0029	–		–	–			CAP. 30pf	
69.									
70.	4400-0043	–		1	1			CAP. 47uf, ±10%, 6V	
71.									
72.	5100-0016	–		–	–			CRYSTAL, 24MHZ	
73.									
74.	6000-0190	–		–	–			HEADER, 8 PIN CONN	
75.									
76.									

GOULD

TITLE ASSEMBLY MPU PWB | LM | DRAWING NO. 0114-0185 | REV V

MODEL | SHEET 9 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
77.	6100-0121	2	–			–		SOCKET 20 PIN	X7L, X8L
78.	6100-0123	1	–			–		SOCKET 40 PIN	X10L
79.	6100-0151	16	–			–		SOCKET 28 PIN	X1A-X1H, X2A-X2H
80.									
81.									
82.	7100-0017	.1	–			–		WIRE CRYSTAL STRAP #22AWG	Y1
83.									
84.									
85.	9000-0054	8	–			–		WIRE, FORMED 16 PIN	GND1 - GND8
86.									
87.									
88.	0120-0085-10	–	–			–		ASSY., 16 PROM SET PROGRAM CODE K20S (REF ITEMS 98 TO 113)	
89.	0114-2020-10	–	–			1		ASSY., PROM K101 CODE (REF ITEMS 98 TO 113)	
90.	0114-2021-10	–	–			–		ASSY, PROM K102 CODE (REF ITEMS 98 TO 113)	
91.	0950-0150-10	–	1			–		ASSY, PROM K500 CODE (REF ITEMS 98 TO 113)	
92.									
93.									
94.									
95.									
96.									

GOULD

TITLE ASSEMBLY MPU PWB | LM | DRAWING NO. 0114-0185 | REV V

MODEL | SHEET 10 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-90	U/M	DESCRIPTION	REFERENCE DESIGNATION
77	6100-0121	–		–	–	–		SOCKET 20 PIN	X7L, X8L
78	6100-0123	–		–	–	–		SOCKET 40 PIN	X10L
79	6100-0151	–		–	–	–		SOCKET 28 PIN	X1A-X1H, X2A-X2H
80									
81									
82	7100-0017	–		–	–	–		WIRE, CRYSTAL STRAP, #22AWG	Y1
83									
84									
85	9000-0054	–		–	–	–		WIRE FORMED 16 PIN	GND1-GND8
86									
87									
88	0120-0085-10	–		–	1	–		ASSY 16 PROM SET PROGRAM CODE K20S (REF ITEMS 98 TO 113)	
89	0114-2020-10	–		–	–	–		ASSY PROM K101 CODE (REF ITEMS 98 TO 113)	
90	0114-2021-10	1		–	–	–		ASSY PROM K102 CODE (REF ITEMS 98 TO 113)	
91	0950-0150-10	–		–	–	–		ASSY PROM K500 CODE (REF ITEMS 98 TO 113)	
92									
93									
94									
95									
96									

GOULD

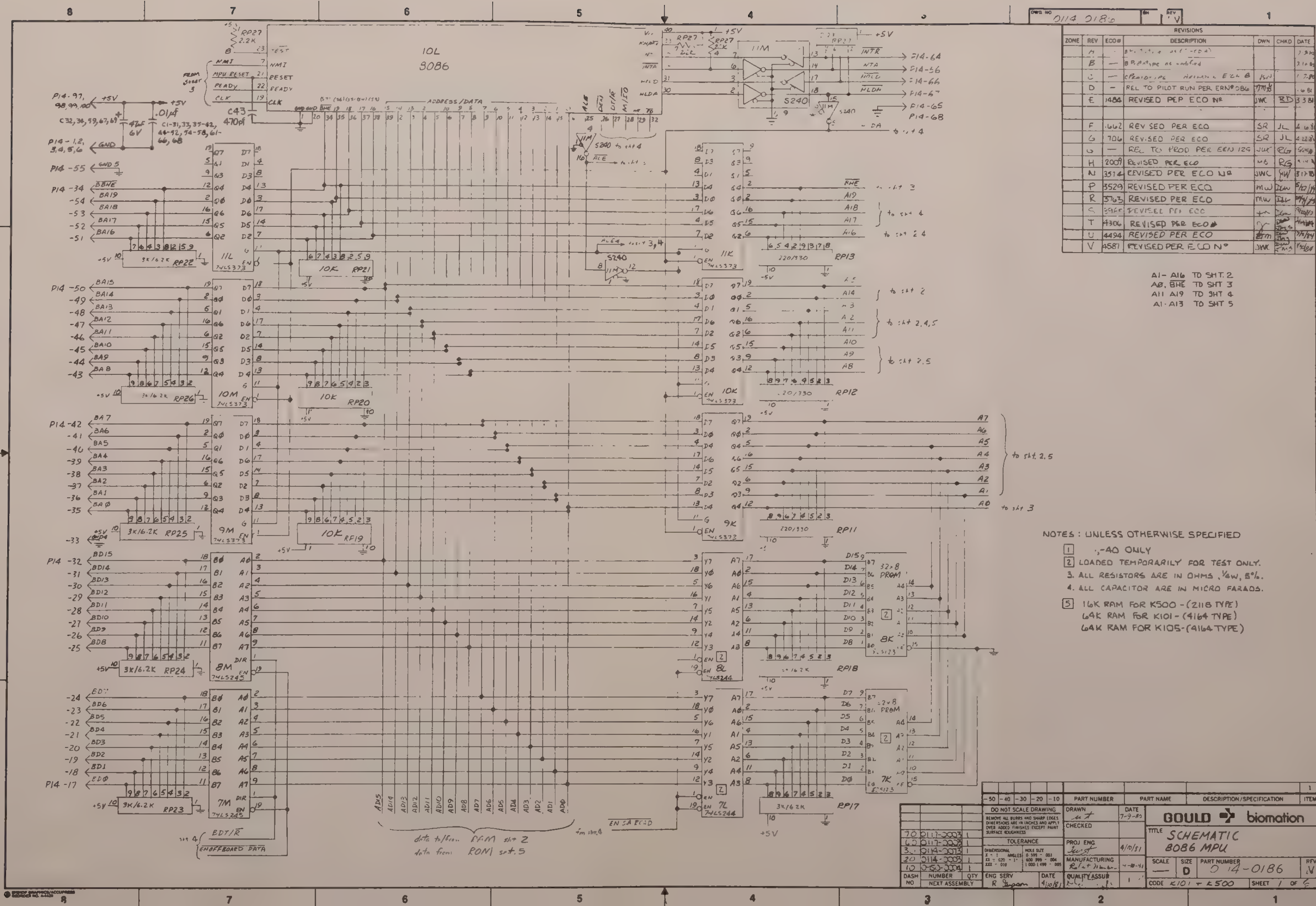
TITLE	LM	DRAWING NO.	REV
ASSEMBLY MPU PWB		0114-0185	V
	MODEL		SHEET 11 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -05	-10	-20	-30	-40	U/M	DESCRIPTION	REFERENCE DESIGNATION
97.	0117-0020-10	–	–			–		ASSY 16 PROM SET PROGRAM CODE (REF ITEMS 98 TO 112)	
98.	1 OF 16	–	REF			REF		PROGRAMMED PROM	2H
99.	2	–							1H
100.	3	–							2G
101.	4	–							1G
102.	5	–							2F
103.	6	–							1F
104.	7	–							2E
105.	8	–							1E
106.	9	–							2D
107.	10	–							1D
108	11	–							2C
109	12	–							1C
110	13	–							2B
111	14	–							1B
112	15	–							2A
113	16 OF 16	–	REF			REF		PROGRAMMED PROM	1A
114									
115									
116									

GOULD

TITLE	LM	DRAWING NO.	REV
ASSEMBLY MPU PWB		0114-0185	V
	MODEL		SHEET 12 OF 12

ITEM NO.	PART NUMBER	QTY PER ASSY -50	-60	-70	-80	-	U/M	DESCRIPTION	REFERENCE DESIGNATION
97.	0117-0020-110	–		1	–			ASSY 16 PROM SET PROGRAM CODE (REF ITEMS 98 TO 112)	
98.	1 OF 16	REF		REF	REF			PROGRAMMED PROM	2H
99.	2								1H
100.	3								2G
101.	4								1G
102.	5								2F
103.	6								1F
104.	7								2E
105.	8								1E
106.	9								2D
107.	10								1D
108.	11								2C
109.	12								1C
110.	13								2B
111.	14								1B
112.	15								2A
113.	16 OF 16	REF		REF	REF			PROGRAMMED PROM	1A
114.									
115.									
116.									



REVISIONS

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	A	—	[illegible]			[illegible]
	B	—	[illegible]			[illegible]
	C	—	[illegible]			[illegible]
	D	—	REL TO PILOT RUN PER ERN# 086			[illegible]
	E	1484	REVISED PER ECO N°	JWC	RD	3 3 81
	F	1662	REVISED PER ECO	SR	JL	[illegible]
	G	706	REVISED PER ECO	SR	JL	[illegible]
	G	—	REL TO PROD PER ERN 129			[illegible]
	H	2009	REVISED PER ECO			[illegible]
	N	3514	REVISED PER ECO N°	JWC		[illegible]
	P	3529	REVISED PER ECO	MW		[illegible]
	R	3763	REVISED PER ECO	MW		[illegible]
	S	3965	REVISED PER ECO			[illegible]
	T	4306	REVISED PER ECO			[illegible]
	U	4494	REVISED PER ECO			[illegible]
	V	4581	REVISED PER ECO N°	JWK		[illegible]

NOTES: UNLESS OTHERWISE SPECIFIED

1. -40 ONLY
2. LOADED TEMPORARILY FOR TEST ONLY.
3. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
4. ALL CAPACITOR ARE IN MICRO FARADS.
5. 16K RAM FOR K500 - (2118 TYPE)
   64K RAM FOR K101 - (4164 TYPE)
   64K RAM FOR K105 - (4164 TYPE)

DO NOT SCALE DRAWING

GOULD biomation

TITLE SCHEMATIC 8086 MPU

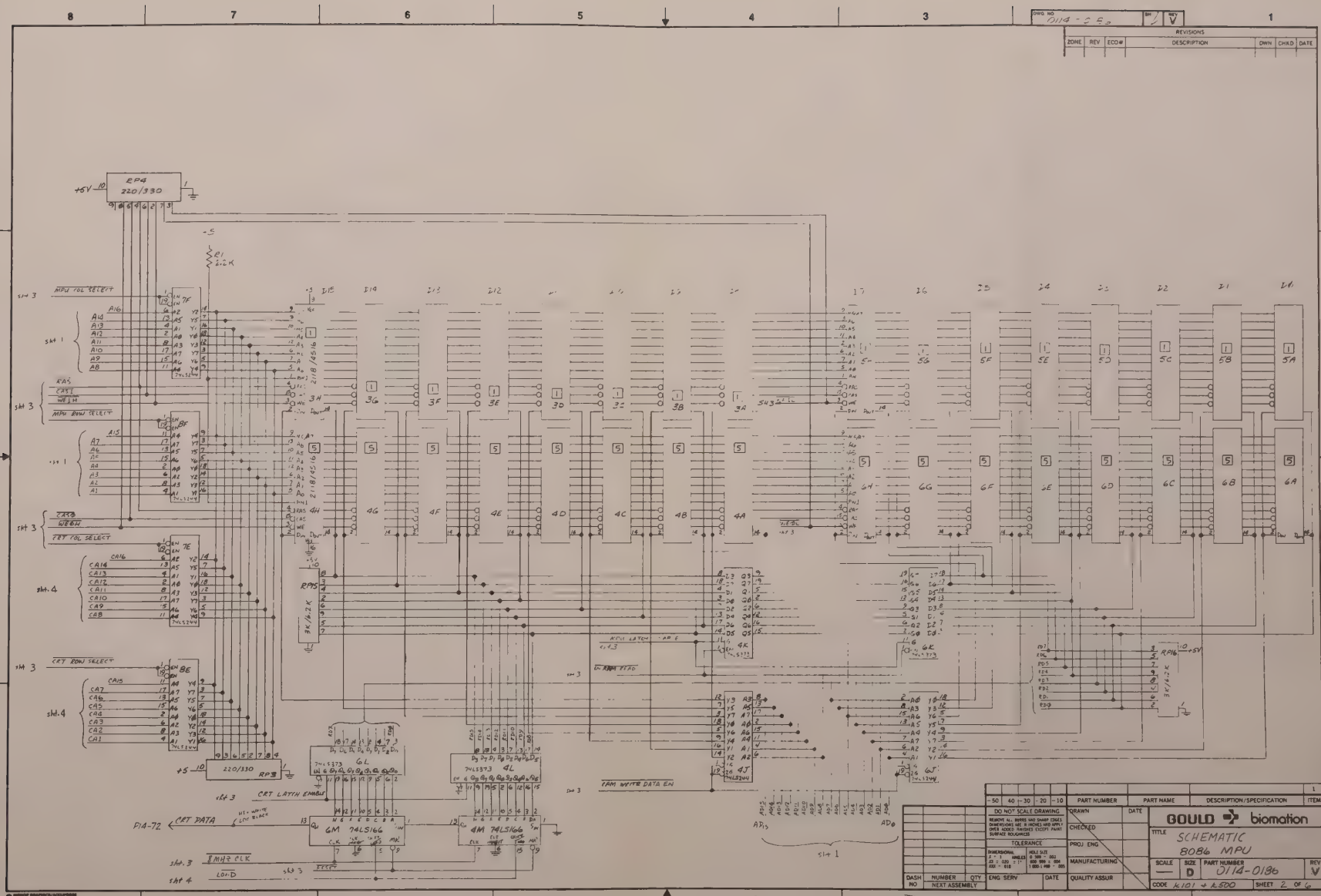
DWG NO 0114-0186 REV V

SIZE D PART NUMBER 0114-0186

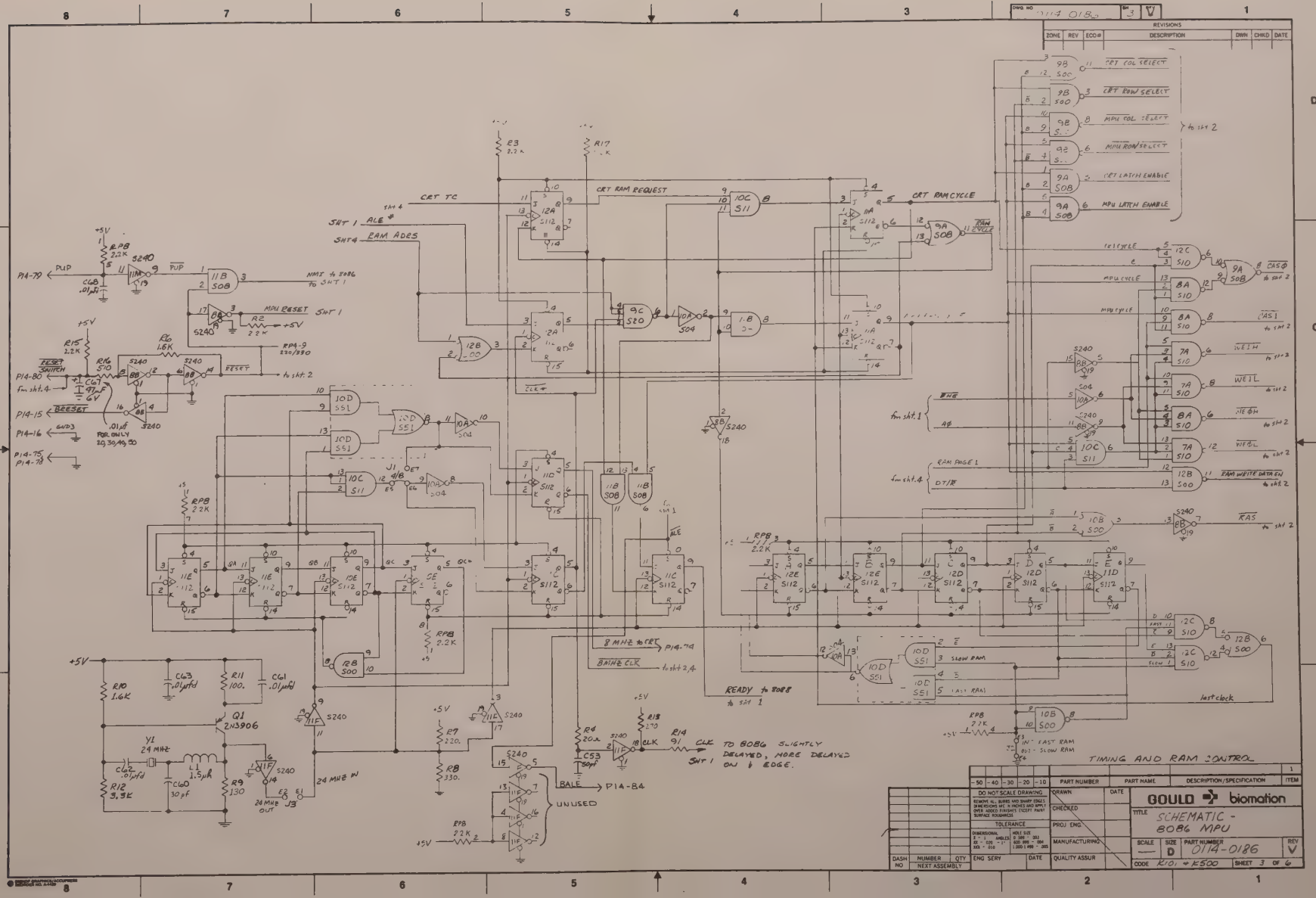
CODE K101 - K500 SHEET 1 OF 5

DATE 7-9-80

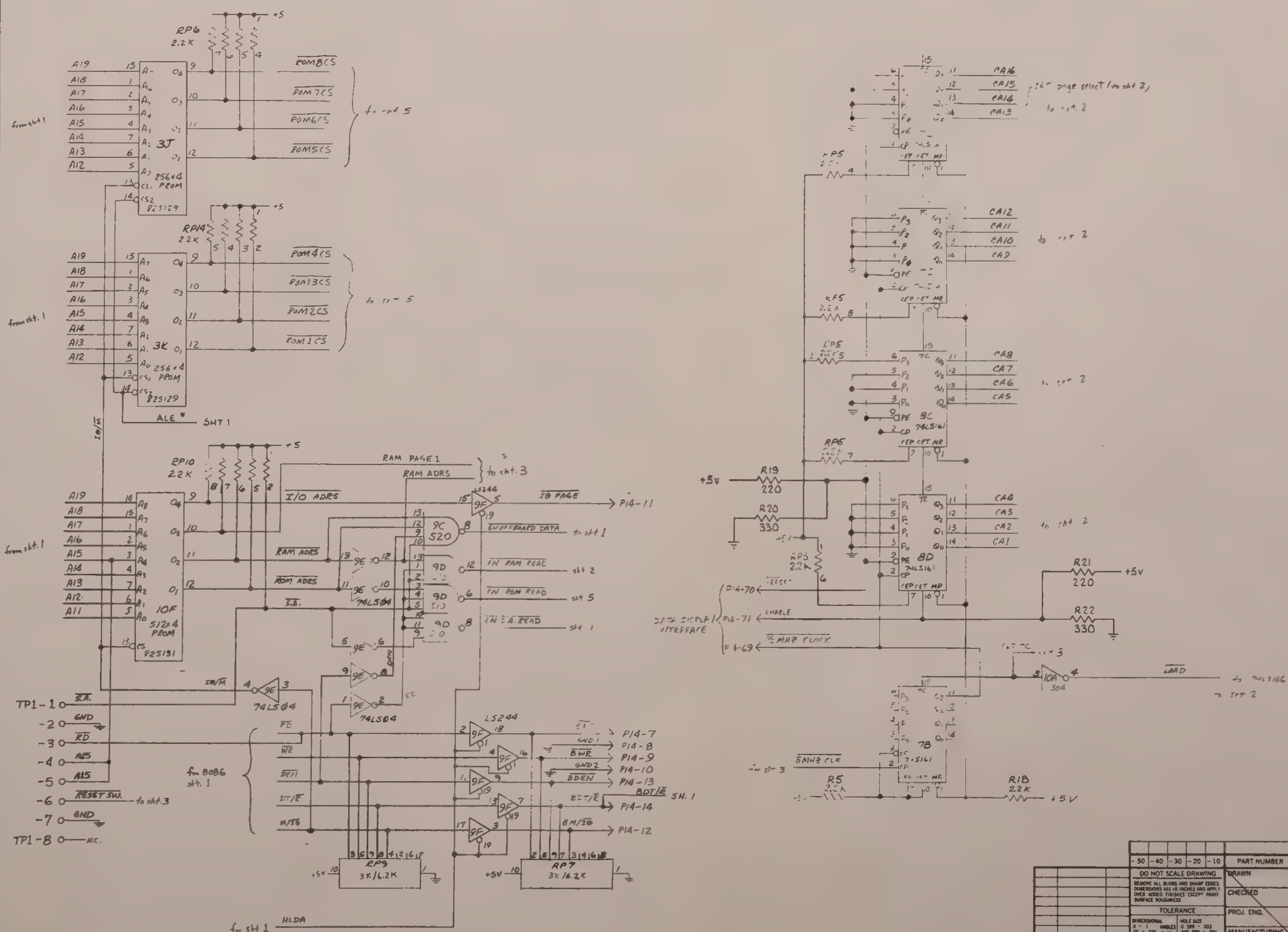
PROJ ENG 4/10/81



RP4
220/330
+5V
R1
2.2K
MPU COL SELECT
MPU ROW SELECT
CRT COL SELECT
CRT ROW SELECT
RP15
3K/6.2K
RP16
3K/6.2K
RP3
220/330
CRT LATCH ENABLE
CRT DATA
P14-72
8MHZ CLK
LOAD
6M 74LS166
4M 74LS166
74LS373
74LS244
RAM WRITE DATA EN
DO NOT SCALE DRAWING
TOLERANCE
DIMENSIONAL
HOLE SIZE
ENG SERV
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
GOULD biomation
TITLE
SCHEMATIC
8086 MPU
SCALE
SIZE
D
PART NUMBER
0114-0186
REV
V
CODE
K101 + K500
SHEET 2 OF 6
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE



CRT TC
CRT RAM REQUEST
CRT RAM CYCLE
CRT COL SELECT
CRT ROW SELECT
MPU COL SELECT
MPU ROW SELECT
CRT LATCH ENABLE
MPU LATCH ENABLE
to sht 2
CRT CYCLE
MPU CYCLE
CAS0
CAS1
WE1H
WE1L
WE0H
WE0L
RAM WRITE DATA EN
RAS
RAM PAGE 1
DT/R
SLOW RAM
FAST RAM
last clock
8 MHZ to CRT
BMHZ CLK
READY to 8088
to sht 1
TO 8086 SLIGHTLY DELAYED, MORE DELAYED ON ↓ EDGE.
BALE
UNUSED
24 MHZ IN
24 MHZ OUT
Y1 24 MHZ
Q1 2N3906
NMI to 8086
MPU RESET
RESET SWITCH
BRESET
GND3
P14-79
P14-80
P14-15
P14-16
P14-75
P14-78
P14-74
P14-84
TIMING AND RAM CONTROL
DO NOT SCALE DRAWING
TOLERANCE
GOULD biomation
TITLE SCHEMATIC - 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV V
CODE K101 + K500
SHEET 3 OF 6



ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE

DWG NO 0114-0186 SH 4 REV V

GOULD biomation

TITLE SCHEMATIC - 8086 MPU

SCALE	SIZE	PART NUMBER	REV
—	D	0114-0186	V

CODE K101 - K500 SHEET 4 OF 6

DO NOT SCALE DRAWING

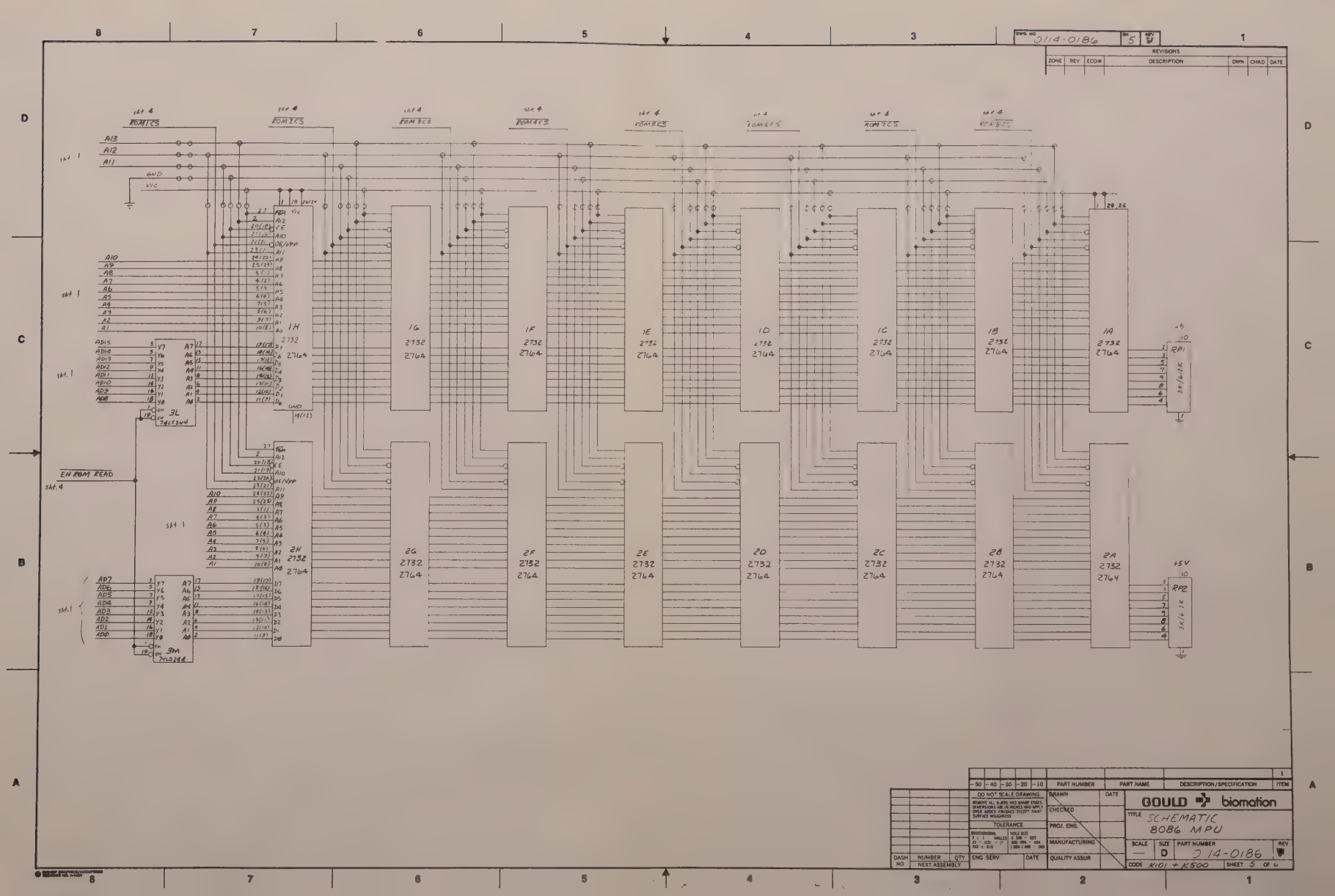
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DRAWN / DATE / CHECKED / PROJ. ENG. / MANUFACTURING / QUALITY ASSUR / ENG. SERV / DATE

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

-50 | -40 | -30 | -20 | -10 | PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITEM



DWG. NO 0114-0186
SH 5
REV
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
ROM1CS
ROM2CS
ROM3CS
ROM4CS
ROM5CS
ROM6CS
ROM7CS
ROM8CS
A13
A12
A11
GND
VCC
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
3L
74LS244
3M
74LS244
EN ROM READ
1H
2732
2764
2H
2732
2764
1G
2732
2764
1F
2732
2764
1E
2732
2764
1D
2732
2764
1C
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1B
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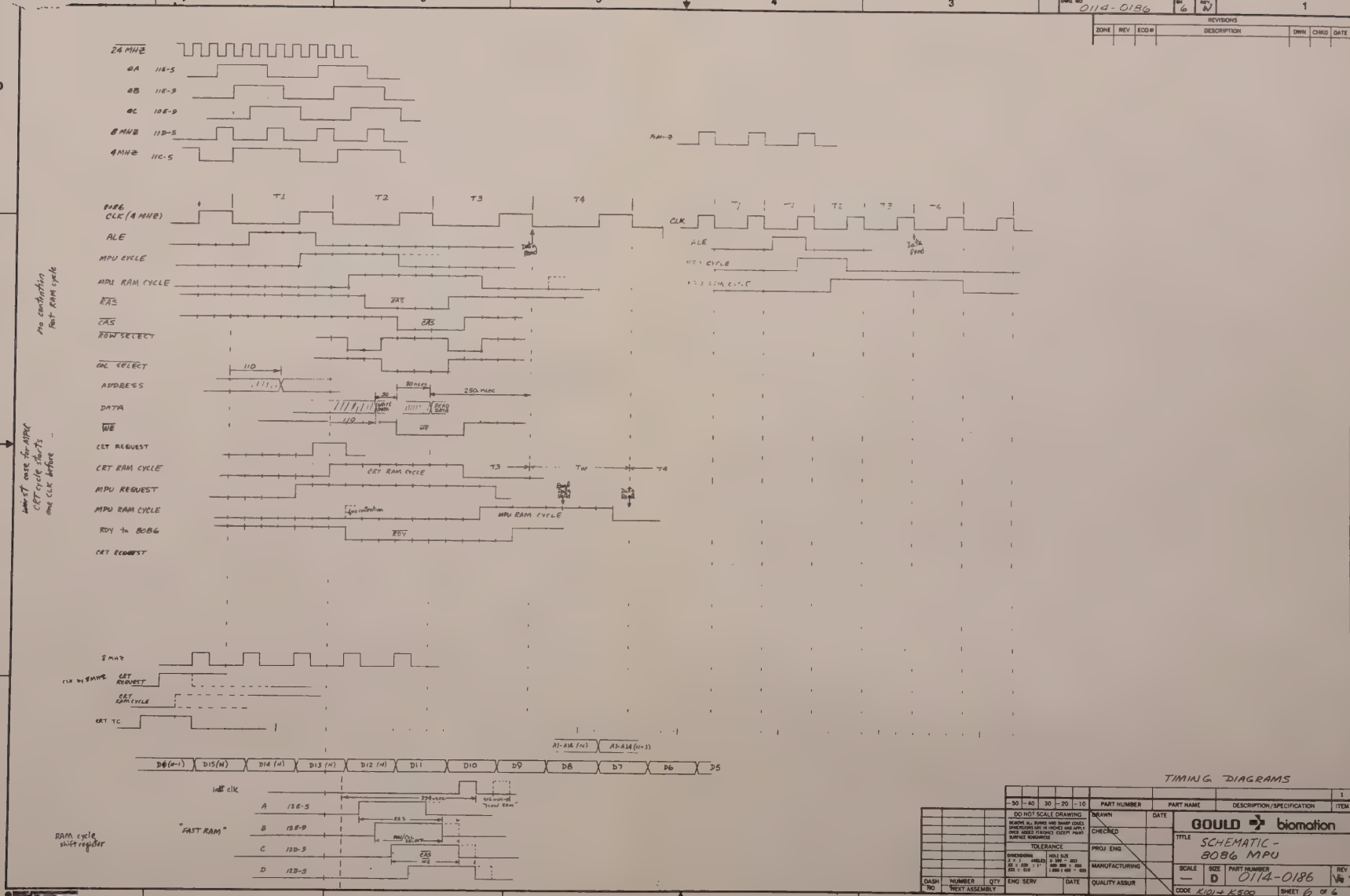
2764
1A
2732
2764
2G
2732
2764
2F
2732
2764
2E
2732
2764
2D
2732
2764
2C
2732
2764
2B
2732
2764
2A
2732
2764
RP1
3K/6.2K
RP2
3K/6.2K
+5V
+5
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
GOULD biomation
TITLE SCHEMATIC 8086 MPU
SCALE
SIZE D
PART NUMBER 0114-0186
REV
CODE K101 + K500
SHEET 5 OF 6



TIMING DIAGRAMS

DWG NO	SH	REV
0114-0186	6	N

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ABOVE FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONS: X ± .1 ANGLES ±1°; XX ± .020 = 1°; XXX ± .010

HOLE SIZE: 0 .188 – .203 .005 .188 = .004 .005 (.400 = .005

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN		DATE
CHECKED		
PROJ ENG		
MANUFACTURING		
QUALITY ASSUR	ENG SERV	DATE

GOULD biomation

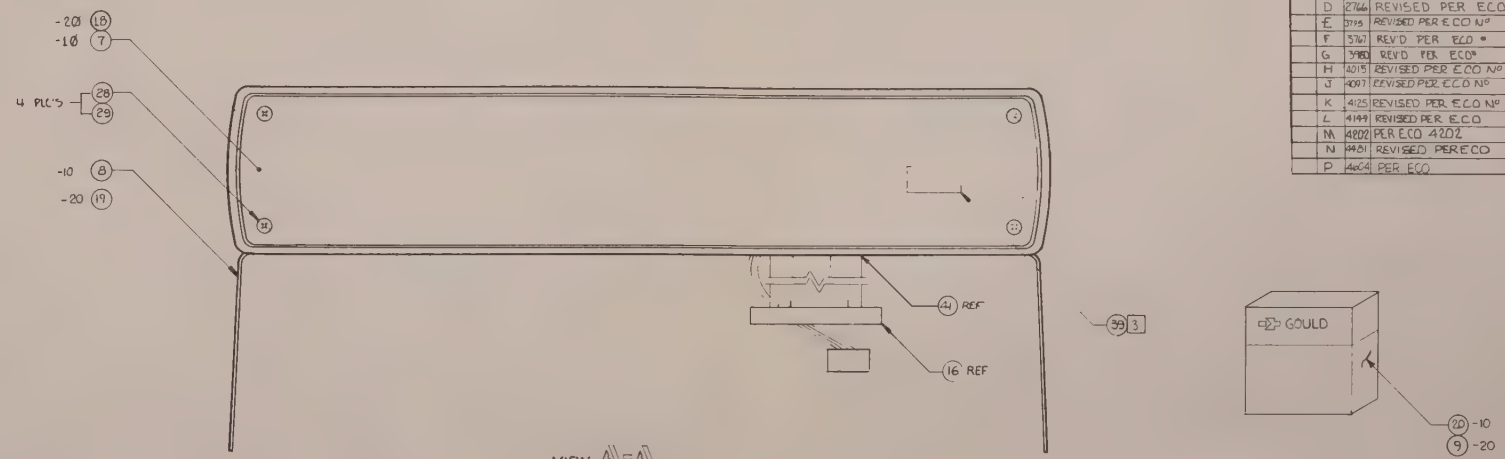
TITLE: SCHEMATIC - 8086 MPU

SCALE	SIZE	PART NUMBER	REV
—	D	0114-0186	N

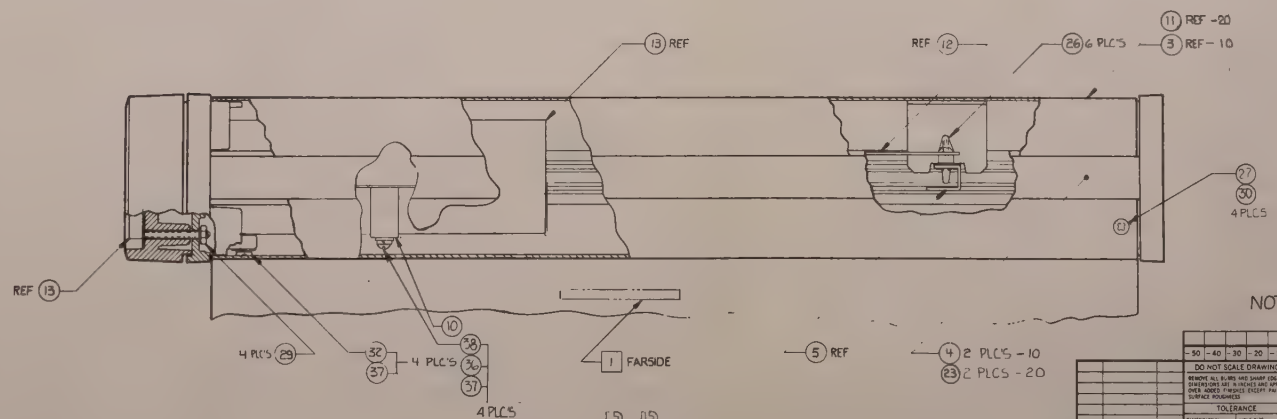
CODE K101+K500 SHEET 6 OF 6

DWG NO 0114-0468 SH 1 REV P

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		REL PER ERN # 272	[illegible]	[illegible]	[illegible]
	B		PER ECO # 2718	[illegible]	[illegible]	[illegible]
	C	2728	REVISED PER ECO Nº	JWC	[illegible]	[illegible]
	C		PROD REL ERN # 287	JWC	[illegible]	[illegible]
	D	2766	REVISED PER ECO #	[illegible]	[illegible]	[illegible]
	E	3795	REVISED PER ECO Nº	JWC	[illegible]	[illegible]
	F	3767	REV'D PER ECO #	STM	[illegible]	[illegible]
	G	3980	REV'D PER ECO#	STM	[illegible]	[illegible]
	H	4015	REVISED PER ECO Nº	JWC	[illegible]	[illegible]
	J	4097	REVISED PER ECO Nº	JWC	[illegible]	[illegible]
	K	4125	REVISED PER ECO Nº	JWC	[illegible]	[illegible]
	L	4149	REVISED PER ECO	JWC	[illegible]	[illegible]
	M	4202	PER ECO 4202	[illegible]	[illegible]	[illegible]
	N	4481	REVISED PER ECO	JWC	[illegible]	[illegible]
	P	4604	PER ECO 7 3 84	[illegible]	[illegible]	[illegible]



VIEW A-A
ROTATED CLOCKWISE 90°



VIEW B-B
ROTATED COUNTER CLOCKWISE 90°

3 TYPE ASSY NO. 0114-0468 APPROPRIATE DASH NO, CURRENT REV LEVEL, AND SERIAL NO.

2 VIEW B-B SHOWS TEAC DRIVES. OTHER APPROVED DRIVES MAY BE USED. BOTH DRIVES MUST BE MFG'D BY THE SAME VENDOR.

1 TYPE ASSY NO. 0114-0468 APPROPRIATE DASH Nº, CURRENT REVISION LETTER AND SERIAL NO

NOTES: UNLESS OTHERWISE SPECIFIED.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL ± 1 ANGLES ± .5 ± .020 ± .1 ± .010
HOLE SIZE 0.500 - .003 .000 .999 - .004 1.000 1.499 .005

DASH NO	NUMBER NEXT ASSEMBLY	QTY
-20	0120-0002	1

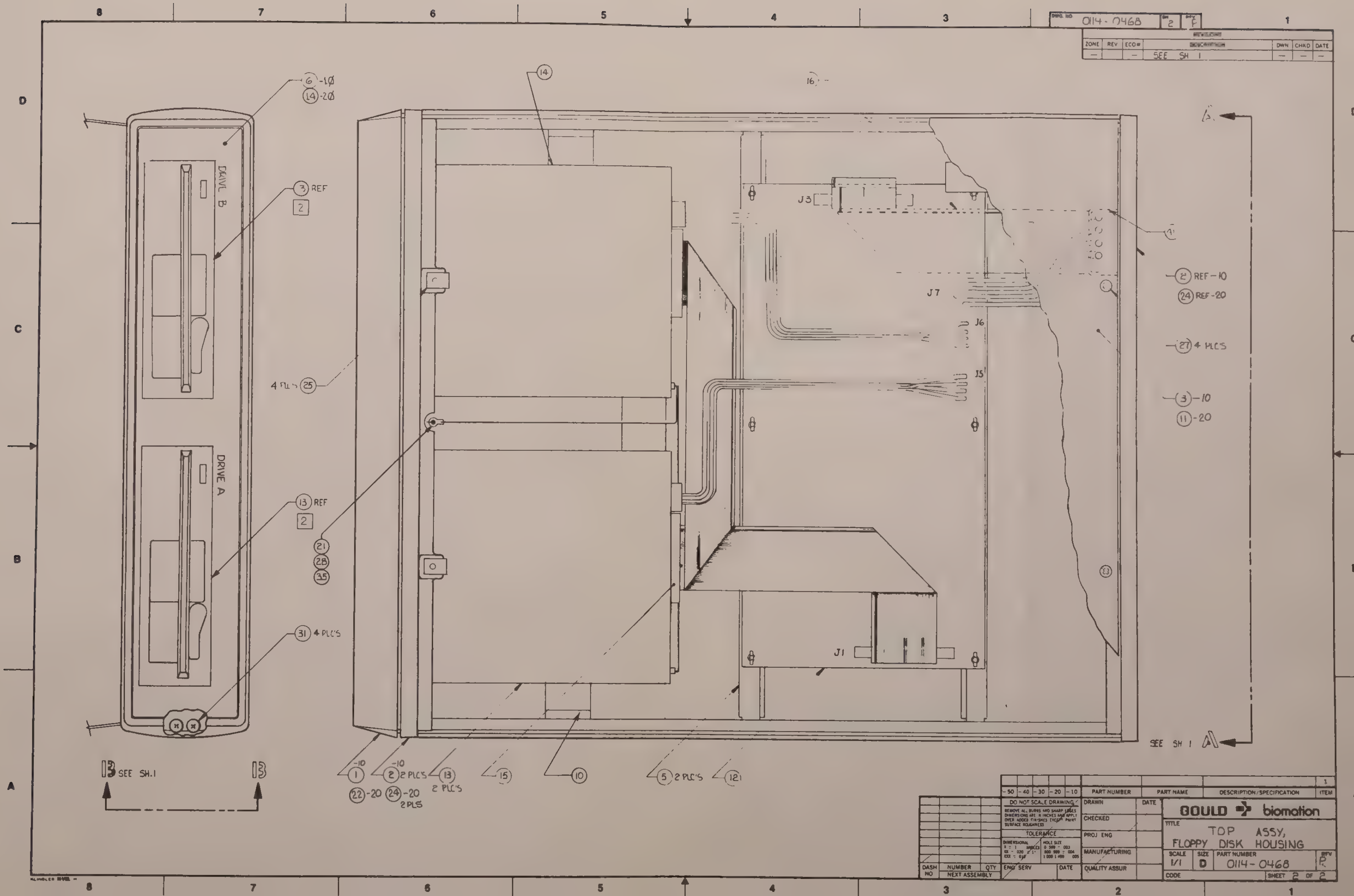
ENG SERV R Gipson DATE 11-2-82
DRAWN [illegible] DATE 4/21/82
CHECKED R Gipson 11/12/82
PROJ ENG [illegible] 4/23/82
MANUFACTURING [illegible] 11/12/82
QUALITY ASSUR [illegible] 11/12/82

GOULD biomation

TITLE TOP ASSY, FLOPPY DISK HOUSING.

SCALE 1/1 SIZE D PART NUMBER 0114-0468 REV P

CODE SHEET 1 OF 2


0114-0468
2
F
ZONE
REV
ECO#
SEE SH 1
DWN
CHKD
DATE
DRIVE B
DRIVE A
3 REF
2
13 REF
2
31 4 PLC'S
6 -10
14 -20
4 PLCS 25
21
28
35
14
16
J3
J7
J6
J5
J1
2 REF -10
24 REF -20
27 4 PLCS
3 -10
11 -20
SEE SH 1
A
B SEE SH.1
B
1 -10
22 -20
2 -10 2 PLCS
24 -20 2 PLS
13 2 PLC'S
15
10
5 2 PLC'S
12
-50
-40
-30
-20
-10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
ENG SERV
DATE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
GOULD biomation
TITLE
TOP ASSY,
FLOPPY DISK HOUSING
SCALE 1/1
SIZE D
PART NUMBER 0114-0468
REV F
CODE
SHEET 2 OF 2

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1								—	1	0114-0462-10	BEZEL, FRONT.		
2								—	2	0114-0463-10	BEZEL, REAR.		
3								—	1	0114-0466-10	COVER, TOP.		
4								—	2	0114-0465-10	SIDE RAIL.		
5								2	2	0114-0469-10	BRKT, PCB SUPPORT.		
6								—	1	0114-0470-20	PANEL, FRONT.		
7								—	1	0117-0169-20	PANEL, REAR.		
8								—	1	0114-0467-10	COVER.		
9								1	—	0120-0079-10	K235 STORAGE OPERATING SYSTEM SOFTWARE SHIPPING ASSY		
10								1	1	0114-0441-10	BRKT FLOPPY DISK SUPPORT		
11								1	—	0114-0466-30	COVER, TOP		
12								1	1	0114-0475-10	STORAGE SYSTEM ASSY. PWB		✓
13								2	2	7500-0003-10	FLOPPY DISK DRIVE		✓
14								1	—	0114-0470-40	PANEL, FRONT		✓
15								1	1	0117-0164-10	CABLE ASSY, SIGNALS FDC TO FLOPPY.		✓
16								1	1	0114-0482-10	CABLE ASSY, SIGNALS KIDI TO FDC.		✓
17													✓
18								1	—	0117-0169-30	PANEL, REAR		
19								1	—	0114-0467-30	COVER		✓
20								—	1	0114-2003-10	SOFTWARE DISK, SHIPPING, ASSY		
21								1	1	0114-0485-10	CABLE ASSY	GND	
22								1	—	0114-0462-30	BEZEL, FRONT		
23								2	—	0114-0465-30	SIDE RAIL		
24								2	—	0114-0463-30	BEZEL, REAR		
25								4	4	7000-0334-10	SPEED N.T. # 6-32 NC		
26								6	6	7000-0461-10	PCB MASTIC SUPPORTS		
27								8	8	7021-2632-12	SCREW, FLAT HD PHILIPS 6-32X3/8 LG SST		

REV	DESCRIPTION	DATE	DWN	CKD
	SEE HISTORY	1-1984	Karen	
M	PER ECO 4202	1-1984	Karen	
N	PER ECO 4481	4-16-84		
P	PER ECO 4604	7-3-84		

DASH NO.	NUMBER	NEXT ASSEMBLY	QTY
-10	0114-2001		1

	DATE
DWN	
CHK RG	11/9/82
ENGR	11/29/82
MFG.	11/29/82
Q.A.	

LIST OF MATERIAL

TOP ASSY,
FLOPPY DISK HOUSING.

GOULD biomation

B | 0114-0468 | REV F

MODEL K101/102 | SHEET 1 OF 2

KLINGLER 8½ x 11

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28								5	5	7011-1632-16	SCREW, PAN-HD. PH. # 6 X 1/2 LG		
29								8	8	7071-1632-00	KEPNUT # 6		
30								4	4	7072-1632-00	HEX NUT NYLON LOCKING #6-32		
31								8	8	7012-1600-20	SCREW THD FORMING 6-32 x 5/8 LG	PHLPS PAN - HD, ELCO, SWAGEFORM OR PARKER TYPE C	
32								4	4	7000-0463-12	SCREW, METRIC, 3mm X 12 mm LG	PHILLIPS HD. 3X12 DIN 7985	
33													
34													
35								1	1	7086-1006-00	#6 STAR WASHER		
36								4	4	7000-0463-08	SCREW 3mmX8mm PHILLIPS HEAD		
37								8	8	7082-1004-00	FLAT WASHER #4 L.P		
38								4	4	7084-0004-10	LOCK WASHER, INT STAR #4		
39								1	1	6303-0040	ABEL, MODEL		
40								33	33	7200-0044-10	GROMMET		
41													
42													
43													
44													
45													
46													
47													
48													
49													
50													
51													
52													
53													
54													

REV	DESCRIPTION	DATE	DWN	CKD
	SEE SHT 1			

DASH NO.	NUMBER	NEXT ASSEMBLY	QTY

	DATE
DWN	
CHK	
ENGR	
MFG.	
Q.A.	

LIST OF MATERIAL

TOP ASSY
FLOPPY DISK HOUSING

GOULD biomation

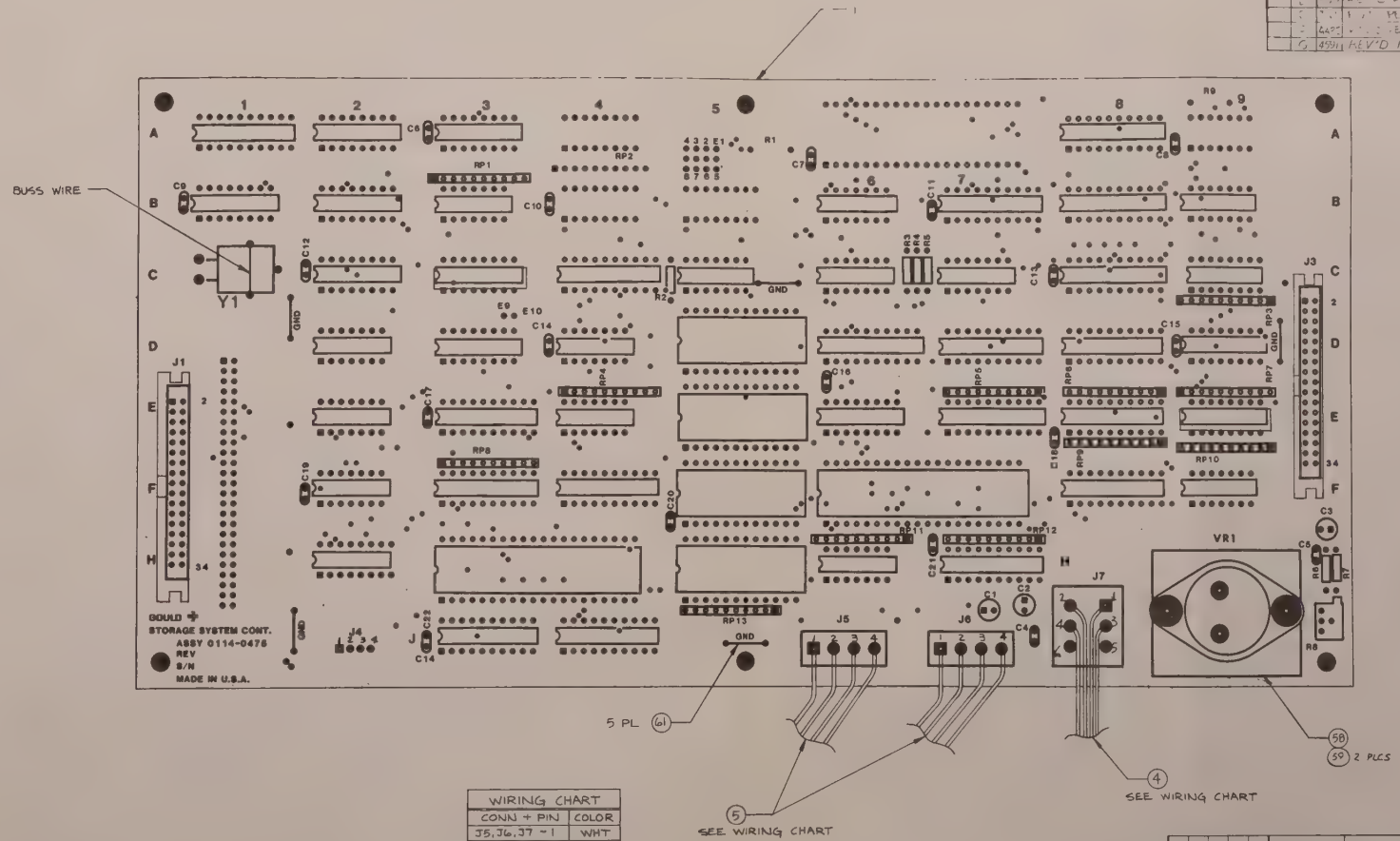
B | 0114-0468 | REV P

MODEL K101/102 | SHEET 2 OF 2

KLINGLER 8½ x 11

DWG NO 0114-0475 SH 1 REV G

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	–	PROTOTYPE	[illegible]		
	B	–	REVISED 7-19-82	[illegible]		
	E	–	REL PER ERN # 275		[illegible]	[illegible]
	C	2104	REVISED PER ECO	[illegible]	[illegible]	
	C		PROD REL ERN 287	HA	[illegible]	
	[illegible]	[illegible]	[illegible] PER ECO	[illegible]	DCW	[illegible]
	[illegible]	[illegible]	[illegible] PER ECO	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible] PER ECO	HW	[illegible]	[illegible]
	G	4591	REV'D PER ECO	RTM	[illegible]	[illegible]



WIRING CHART	
CONN + PIN	COLOR
J5, J6, J7 - 1	WHT
J5, J6, J7 - 2	BLK
J5, J6, J7 - 3	BLK
J5, J6, J7 - 4	RED

-50	40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL ± 1 ANGLES ± 1/2° HOLE SIZE ± .003 .XX ± .020 .XXX ± .010 .XXX ± .005 .XXX ± .010 .XXX ± .005

DASH NO	NUMBER	QTY
-10	0114-0468	1
	NEXT ASSEMBLY	

ENG SERV [illegible] DATE [illegible]

DRAWN [illegible] DATE 7/7/82
CHECKED [illegible] 11/12/82
PROJ ENG [illegible] 11/12/82
MANUFACTURING [illegible] 11/12/82
QUALITY ASSUR. [illegible] 11/12/82

GOULD biomation

TITLE ASSEMBLY – STORAGE SYSTEM CONTROLLER

SCALE 2/1 SIZE D PART NUMBER 0114-0475 REV G

CODE SHEET 1 OF 1

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	0114-0477	PWB		
2									1	0114-0474	I.C. PROM 32x8	3C	
3									1	0114-0479	I.C. PROM 256x4	9E	
4									1	0114-0429	Cable Assy, Power IN	J7	
5									2	0114-0481	Cable Assy. FDC to Floppy	J5, J6	
6									1	1700-0109	I.C. LM350K 3 AMP	VR1	
7									2	1800-0085	I.C 7407 HEX O.C. BUFFER	2E, 2F	
8									1	-0097	I.C. 7406 HEX O.C. INVERTER	2D	
9													
10									1	-0106	I.C. 74LS02 QUAD 2-IN NOR	5C	
11									2	-0109	I.C 74LS08 QUAD 2-IN AND	7C, 6B	
12									1	-0110	I.C. 74LS10 TRIPLE 3-IN NAND	9F	
13									4	-0115	I.C. 74LS74 DUAL D FLIP-FLOP	6C, 4E, 4D, 3B	
14									2	-0125	I.C. 74LS161 4 BIT COUNTER	,3A, 2C	
15									1	-0181	I.C. 74LS151 8-IN MUX	3D	
16									3	-0193	I.C. 74LS138 1 OF 8 DECODER	6E, 9C, 9D	
17									1	-0216	I.C. 74LS32 QUAD 2-IN OR	6H	
18									2	-0217	I.C. 74LS153	2A, 2B	
19									4	-0231	I.C. 74LS273 OCTAL REGISTER	8D, 8C, 3E, 4C	
20									1	-0237	I.C. 74LS139 DUAL 1 OF 4 DECODER	2H	
21									3	-0240	I.C. 74LS244 OCTAL BUFFER	6D, 8A, 8B	
22									3	-0267	I.C 74LS240 OCTAL INVERTER	7B, 3F, 4F	
23									3	-0268	I.C 74LS245 OCTAL BI-DIR BUFFER	8F, 8E, 7D	
24									1	-0293	I.C. 74LS374 OCTAL REGISTER	7H	
25									1	-0298	I.C. 74LS373 OCTAL LATCH	7E	
26									1	1800 -0311	I.C 7438 QUAD O.C. NAND	9B	
27													

REV	DESCRIPTION	DATE	DWN	CKD
—	SEE HISTORY	—	—	—
G	REV'D PER ECO 4591	6-27-84	R.Tim	Paul Jones

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-10	0114-0468	1

		DATE
DWN	Curt	5-25-82
CHK	Curt	11-12-82
ENGR	Curt	11-12-82
MFG.	P. Strassman	11/12/82
Q.A.	Ron Kuhl	11-12-82

LIST OF MATERIAL

PWB ASSEMBLY

STORAGE SYSTEM I CONTROLLER

GOULD biomation

B | 0114-0475 | REV G

MODEL | SHEET 1 OF 3

KLINEBLER

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28									1	1800-0342	I.C. 8272 FLOPPY CONT.	3H	
29									1	1800-0357	I.C 74LS629 OSCILLATOR	1B	
30									1	1800-0358	I.C 8257-5 DMA CONT.	6F	
31													
32													
33													
34									2	1820-0080	I.C. 6116LA-3 2KX8 RAM	5F, 5H	
35													
36													
37									1	3000-1001	RESISTOR, 1K, 1/4W, 5%	R7	
38									4	3000-2201	RESISTOR 2.2K, 1/4W, 5%	R2-5	
39									1	3000-6806	RESISTOR 680Ω, 1/4W, 5%	R6	
40									1	3300-0092	POT. , 100.Ω, 12 T	R8	
41									8	3700-0049	R. PACK 3K/6.2K, 10 PIN, 8 RES	RP3, 5, 6, 9-13	
42									3	3700-0083	R. PACK 2.2K, 10 PIN, 9 RES	RP1, 4, 7	
43									1	3700-0100	R. PACK 150Ω, 10 PIN, 9 RES	RP8	
44													
45									18	4010-0103	CAP .01 μd, 50 V, 10%	C4-22	
46									1	4400-0043	CAP 47 μf/6 V	C1	
47									2	4400-0045	CAP 33 μf/25 V	C2, 3	
48													
49									1	5100-0021	CRYSTAL, 16. MHZ	Y1	
50													
51													
52									2	6000-0574	CONNECTOR, 34 PIN HEADER	J1, J3	
53													
54									4	6100-0122	SOCKET, 24 PINS	X5D, X5E, X5F, X5H	
55									2	6100-0123	SOCKET, 40 PINS	6F, 3H	
56									2	6100-0120	SOCKET, 16 PIN DIP, LP	3C, 9E	
57													

NOTES

LIST OF MATERIAL

GOULD biomation

B | 0114-0475 | REV G

MODEL | SHEET 2 OF 3

ITEM	QUANTITY PER ASSEMBLY -80	-60	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
58									1	7000-0460-20	HEATSINK, TO-3, Bottom	for VR1	
59									2	7071-0632-00	KEPNUT, 6-32		
60													
61									5	9000-0054	WIRE, FORMED GND POINT		

NOTES

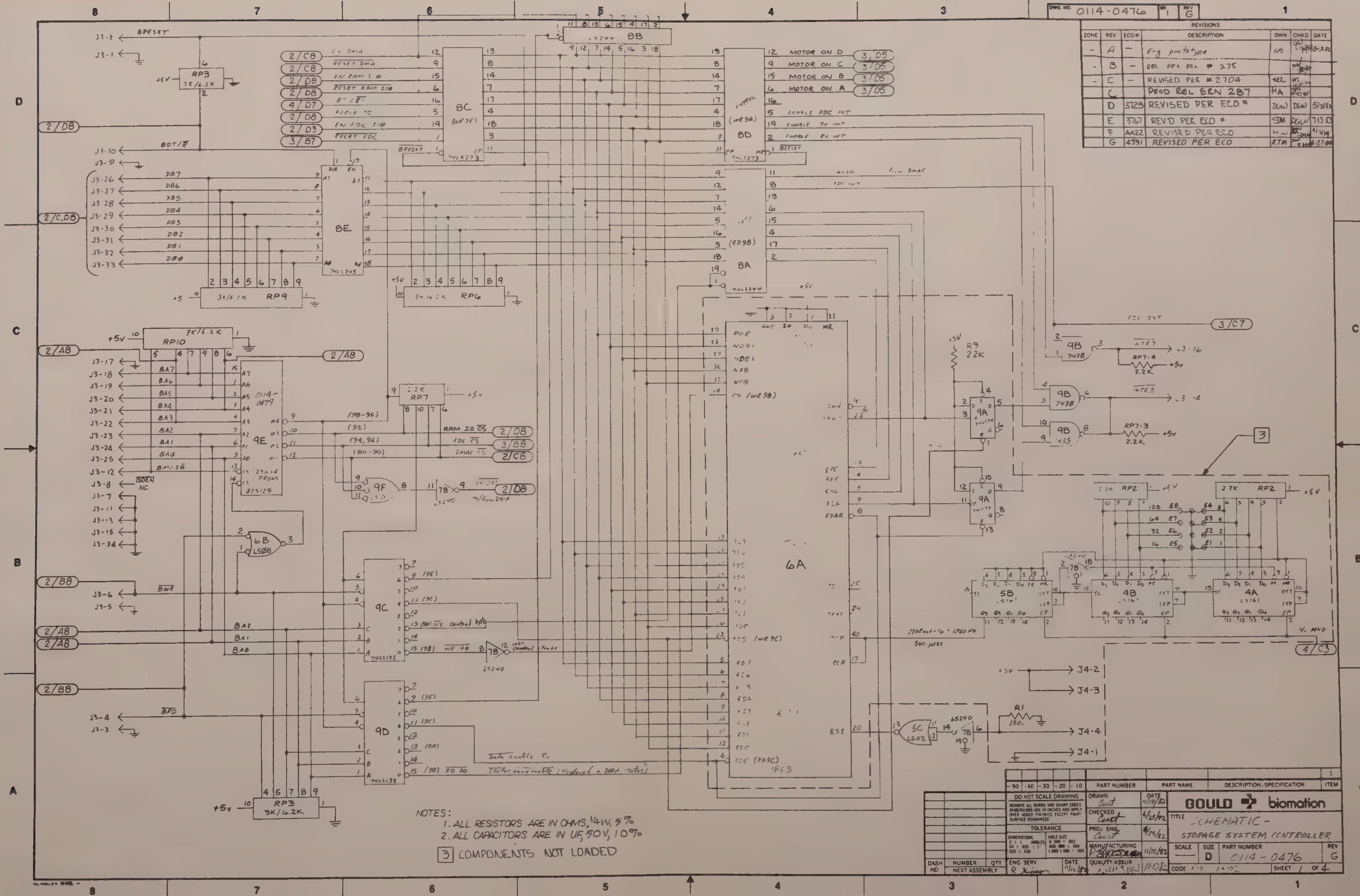
LIST OF MATERIAL

GOULD ▷ biomation

B | 0114-0475 | REV G

MODEL | SHEET 3 OF 3

KLINDLER B-VEL M-10



NOTES:
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITORS ARE IN UF, 50V, 10%
[3] COMPONENTS NOT LOADED

DWG. NO. 0114-0476 SH 1 REV G

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
-	A	—	Eng prototype	LB		
-	B	—	REL PER ERN # 275			
-	C	—	REVISED PER # 2704			
	C		PROD REL ERN 287	HA		
	D	3729	REVISED PER ECO #	DLW	DLW	
	E	3767	REV'D PER ECO #	SJM		
	F	4422	REVISED PER ECO			
	G	4591	REVISED PER ECO	RTM		

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

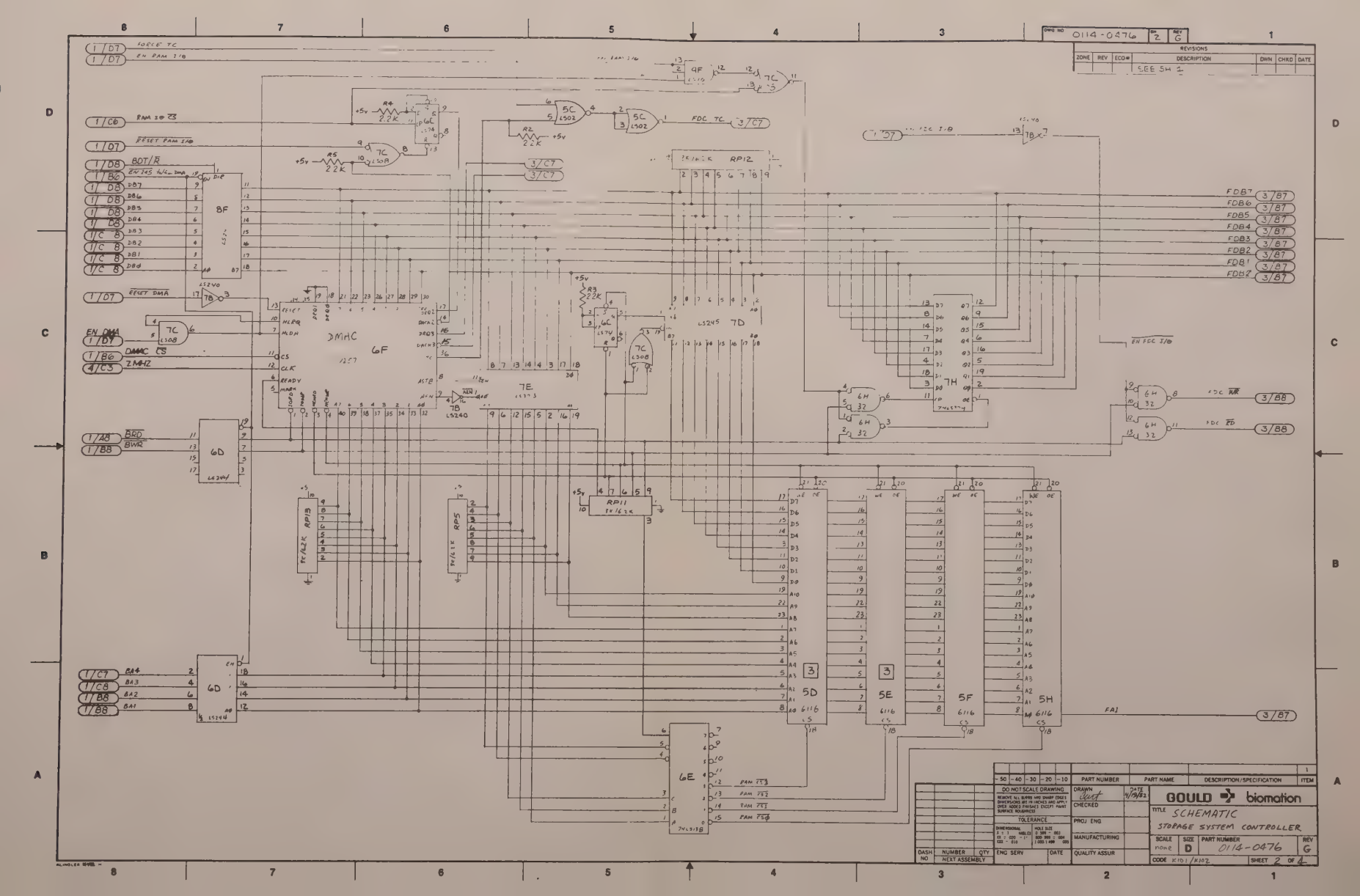
DRAWN Curt 4/19/82
CHECKED Curt 6/25/82
PROJ ENG Curt 6/25/82
MANUFACTURING 11/12/82
QUALITY ASSUR 11-12-82
ENG SERV R. 11/12/82

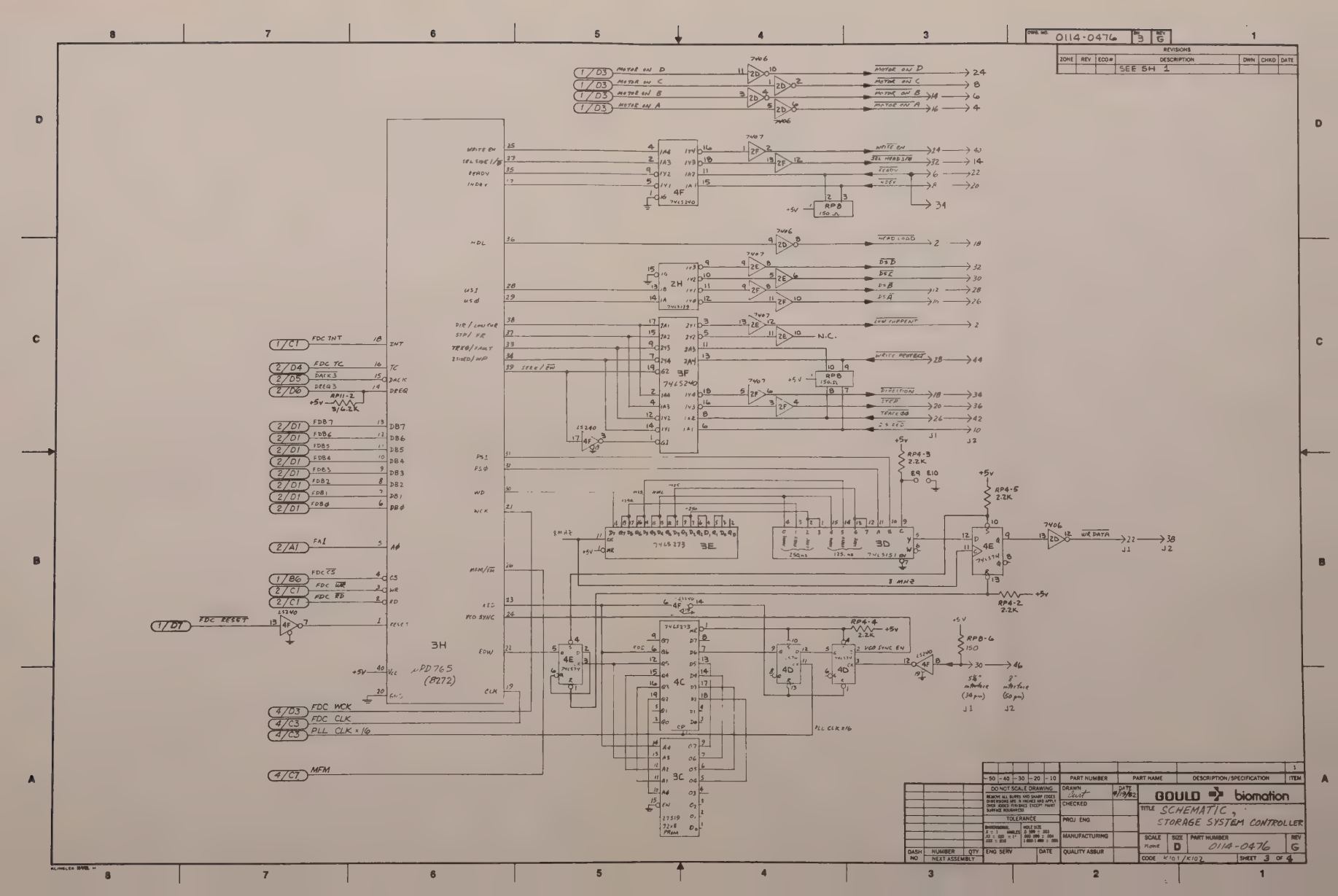
GOULD biomation

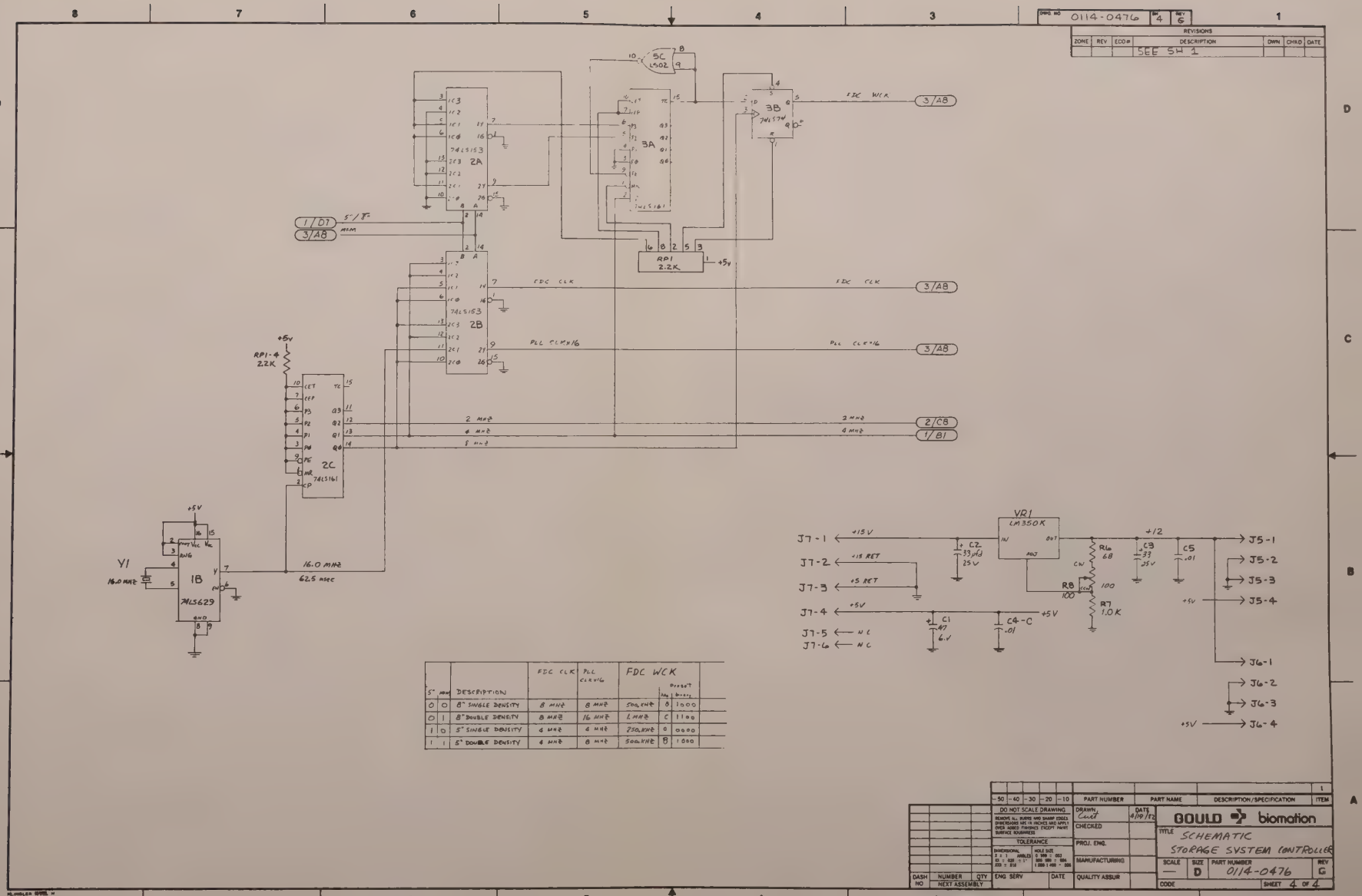
TITLE SCHEMATIC - STORAGE SYSTEM CONTROLLER

SCALE — SIZE D PART NUMBER 0114-0476 REV G

SHEET 1 OF 4


DWG NO 0114-0476
REV G
SHEET 2
REVISIONS
SEE SH 2
FORCE TC
EN RAM I/O
RAM CS
RESET RAM I/O
BOT/R
EN 745 W/L DMA
RESET DMA
EN DMA
DMAC CS
ZMHZ
BRD
BWR
BA4
BA3
BA2
BA1
FDC TC
RAM FD3
RAM FD2
RAM FD1
RAM FD0
FDB7
FDB6
FDB5
FDB4
FDB3
FDB2
FDB1
FDB0
EN FDC I/O
FDC WR
FDC RD
FA1
DMAC
6F
6D
6E
7E
7D
7H
5D
5E
5F
5H
RP12
RP11
RP13
RP5
DMA CLOCK
DO NOT SCALE DRAWING
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
ENG SERV
QUALITY ASSUR
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
GOULD biomation
TITLE SCHEMATIC
STORAGE SYSTEM CONTROLLER
SCALE none
SIZE D
PART NUMBER 0114-0476
REV G
CODE K1D1/R1D2
SHEET 2 OF 4


DWG NO. 0114-0476
SH 3
REV G
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SH 1
MOTOR ON D
MOTOR ON C
MOTOR ON B
MOTOR ON A
WRITE EN
SEL HEAD 1/B
READY
INDEX
HDL
HEAD LOAD
DS D
DS C
DS B
DS A
LOW CURRENT
N.C.
WRITE PROTECT
DIRECTION
STEP
TRACK 00
DS SEL
WR DATA
FDC INT
FDC TC
DACK 3
DREQ 3
FDB 7
FDB 6
FDB 5
FDB 4
FDB 3
FDB 2
FDB 1
FDB 0
FAI
FDC CS
FDC WR
FDC RD
FDC RESET
FDC WCK
FDC CLK
PLL CLK ÷16
MFM
μPD765 (8272)
74LS240
74LS374
74LS273
74LS157
74LS153
74LS32
74LS139
74LS240
74LS74
74LS04
74LS00
74LS86
74LS123
74LS373
74LS374
74LS157
74LS153
74LS32
74LS139
74LS240
74LS74
74LS04
74LS00
74LS86
74LS123
74LS373
27S19 32x8 PROM
RP4-3 2.2K
RP4-5 2.2K
RP4-2 2.2K
RP4-4 2.2K
RP8 150Ω
RP8-6 150
5¼" interface (34 pin)
8" interface (50 pin)
VCO SYNC EN
PLL CLK ÷16
GOULD biomation
TITLE SCHEMATIC, STORAGE SYSTEM CONTROLLER
SCALE none
SIZE D
PART NUMBER 0114-0476
REV G
CODE K101/K102
SHEET 3 OF 4
DO NOT SCALE DRAWING
TOLERANCE
DRAWN Scott
DATE 11/3/82
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DASH NO
NUMBER
NEXT ASSEMBLY
QTY



5"	MFM	DESCRIPTION	FDC CLK	PLL CLK×16	FDC WCK	Preset Mag	Preset Binary
0	0	8" SINGLE DENSITY	8 MHZ	8 MHZ	500 KHZ	B	1000
0	1	8" DOUBLE DENSITY	8 MHZ	16 MHZ	1 MHZ	C	1100
1	0	5" SINGLE DENSITY	4 MHZ	4 MHZ	250 KHZ	0	0000
1	1	5" DOUBLE DENSITY	4 MHZ	8 MHZ	500 KHZ	B	1000

DWG NO 0114-2010 SH 1 REV J

ZONE	REV	ECO #	[illegible]	DWN	CHKD	DATE
	A		PRODUCT REL PER ECN # 295	JC	[illegible]	
	B		PRODUCTION RELEASE PER ECN 300	[illegible]		
	C	3684A	REV'D PER ECO	MW	DCW	[illegible]
	D	3865	REVISED PER ECO	MW	DCW	[illegible]
	E	3906	REVISED PER ECO	MW	DCW	[illegible]
	F	4147	REVISED PER ECO	MW	[illegible]	[illegible]
	G	4425	REVISED PER ECO	JG	[illegible]	[illegible]
	H	4562	REVISED PER E C O N°	JWL	[illegible]	[illegible]
	J	4639	PER ECO	[illegible]	[illegible]	[illegible]

JUMPER	AS ETCHED	-20 K101 K102	-30 K106	-40 K205	-10 K500	DESCRIPTION
E1 TO E2	OUT				JUMPER FOR 50HZ ONLY	CRT SCAN RATE IN-50HZ OUT-60HZ
E3 TO E4	OUT					NOT USED
E5 TO E6	OUT					NOT USED
E7 TO E8	OUT				JUMPER	IN = K500 HORIZ SCAN OUT-K101
E9 TO E10	OUT					A18
E11 TO E12	IN					A17
E13 TO E14	IN					A16
E15 TO E16	IN					A15 } K101 CMOS RAM
E17 TO E18	IN					A14 ADDRESS SELECTION
E19 TO E20	IN					A13
E21 TO E22	IN					A12
E23 TO E24	IN					A19
E25 TO E26	IN					A8 } K500 MEM MAPPED I/O
E27 TO E28	IN					A7 } ADDRESS DECODE
E29 TO E30	IN				CUT	IN SELECTS I/O MAPPED I/O (K101)
E30 TO E31	OUT				JUMPER	IN SELECTS MEM MAPPED I/O (K500)
E32 TO E33	IN				CUT	IN FOR K101
E33 TO E34	OUT				JUMPER	IN FOR K500

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO	NUMBER (NEXT ASSEMBLY)	QTY
-40	0120-0004	1
-30	0117-0003	
-20	0114-0002	
-20	0114-0002	1
-10	0950-0002	1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

ENG SERV | DATE

		DATE
DRAWN	[illegible]	3/26/82
CHECKED	[illegible]	12/0/82
PROJ ENG	[illegible]	1/26/83
MANUFACTURING	[illegible]	1/27/83
QUALITY ASSUR	[illegible]	1/27/83

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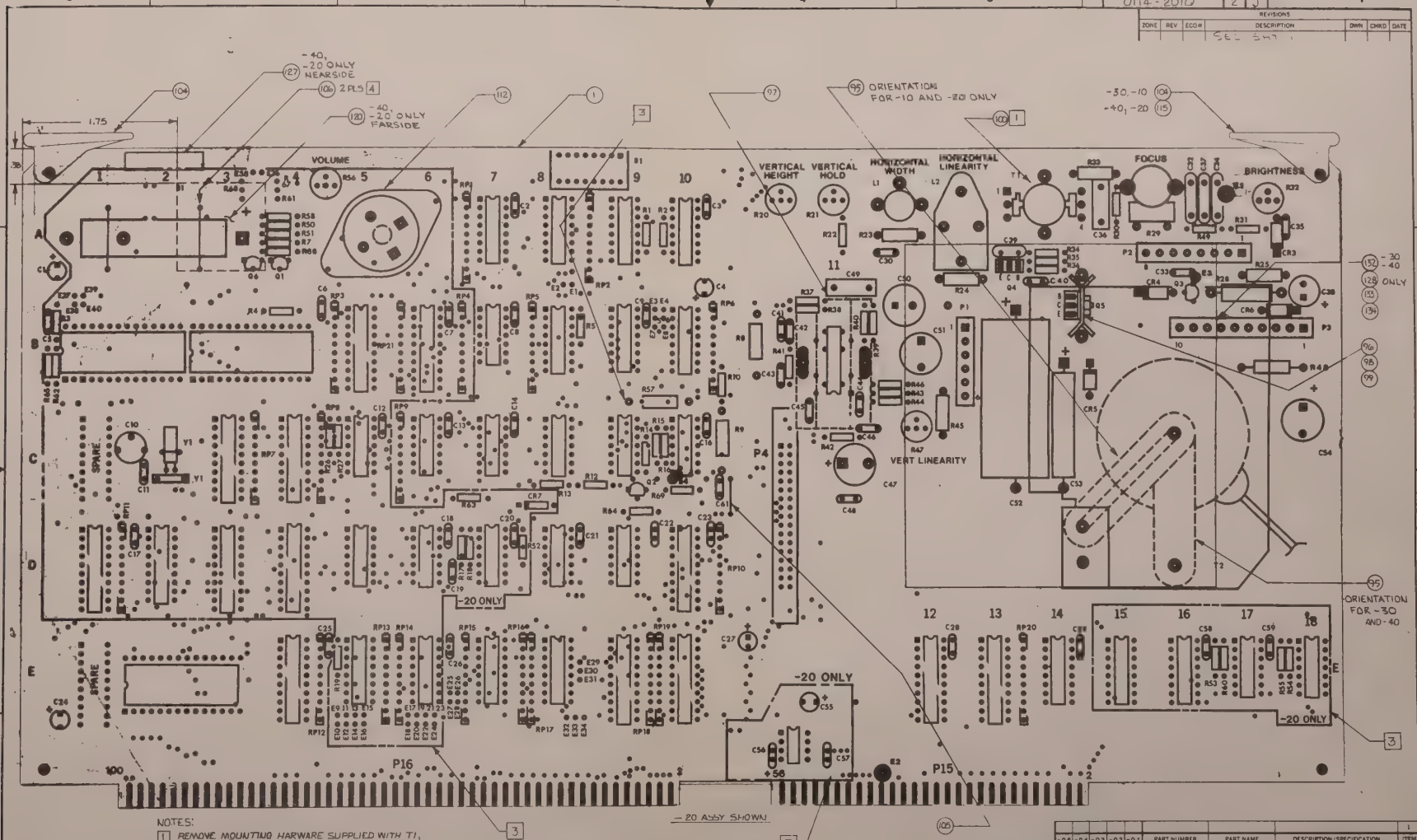
TITLE ASSEMBLY DATA DISPLAY BD

SCALE	SIZE	PART NUMBER	REV
2/1	D	0114-2010	J

CODE K101 / K500 SHEET 1 OF 2



NOTES:

1. REMOVE MOUNTING HARWARE SUPPLIED WITH T1, USE ITEM 100 TO SECURE TO BOARD
2. IC'S 7E, 9E, RP2 & S1 ARE -10; IC 9E & RP2 ARE -30.
3. COMPONENTS IN THIS AREA PLUS R57 ARE -20, -40 ONLY EXCEPT FOR R26 & R27.
4. SECURE BATTERY, B1, TO BOARD WITH ITEM 106 2 PLACES BEFORE SOLDERING LEADS TO PREVENT STRAIN ON BATTERY LEADS.
5. JUMPER FROM E1 TO E2 AND E3 TO E4 ON SOLDER SIDE OF BOARD USE 16AWG 19 STRAND WIRE. MAKE JUMPERS AS SHORT AS POSSIBLE.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES .XX ± .025 ± 1° .XXX ± .010 HOLE SIZE: 0 .599 ± .003 .600 .999 ± .004 1.000 1.499 ± .005

DRAWN: J W CARROLL DATE: 12-6-82

CHECKED: 12/6/82

PROJ ENG

MANUFACTURING

QUALITY ASSUR

ENG SERV

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

GOULD Instruments Division Santa Clara Operations

TITLE: ASSEMBLY DATA DISPLAY BOARD

SCALE: 2/1 | SIZE: D | PART NUMBER: 0114-2010 | REV: J

MODEL | SHEET 2 OF 2

K205 K105, K101, K500

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
1			1	1	1	1	0114-2012	PWB				
2			3	2	3	2	3000-2000	RESISTOR	R35, 36 [1] R64		200Ω, ¼W, 5%	
3			1	1	1	1	3000-3307	RESISTOR	R38		3.3Ω, ¼W, 5%	
4			2	2	2	2	3050-4700		R8,9		470Ω, ½W, 5%	
5			1	1	1	1	3000-8206		R12		82Ω, ¼W, 5%	
6			2	2	2	2	-4700		R5, 34		470Ω	
7			12	2	12	2	-2201		[2] R1, 2 [1] R19, 1, 2, 53-55, 58, 3, 4, 60, 62, 65		2.2K	
8			4	—	4	—	-1002		R17, 18, 52, 63		10K	
9			1	1	1	1	-5601		R46		5.6K	
10			2	2	2	2	-8201		R39, 40		8.2K	
11			2	2	2	2	-4702		R43, 44		47K	
12			1	1	1	1	-1203		R22		120K	
13			2	2	2	2	-2203		R37, 41		220K	
14			1	1	1	—	-2703		R42		270K	
15			1	1	1	1	-5103		R31		510K	
16			—	—	—	1	-6803		R42		680K	
17			2	2	2	2	3000-1004	RESISTOR	R30, 49		1MEG Ω, ¼W, 5%	
18			1	1	1	1	3050-2200	RESISTOR	R24		220Ω, ½W, 5%	

[1] USED ON -20 AND -40

[2] USED ON -10 ONLY

-10 K500

-20 K101/K102

-30 K105

-40 K205

[3] -10-30

ASSEMBLY TIME	COMPONENT LEAD SPACING
	¼W RES -.40 ⅛W RES -.40 ½W RES -.50 1W RES -.70

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	PROD. REL PER ERN # 295 # 302	7/9/82	M.W.		
B	"	7/9/82			
C	REVISED PER ECO # 3684A	5/16/83	MW	DGW	5/16/83
D	REVISED PER ECO # 3865	7/28/83	MW	DGW	8/1/83
E	REVISED PER ECO # 3906	9/23/83	MW	DGW	8/1/83
F	REVISED PER ECO # 4147	11/22/83	MW	DGW	11/22/83
G	REVISED PER ECO # 4425	3-14-84	J.G.	TK	3/14/84

DASH NO.	NUMBER	QTY
-40	0120-0004	1
-20	0114-1002	1
-30	0117-0203	1
-20	0114-0002	1
-10	0950-0002	1

NEXT ASSEMBLY

DRAWN M.W. DATE 11/8/82
CHECKED 11/9/82
ENGINEER 11/26/83
MANUFACTURING 1/27/83
QUALITY ASSURANCE 1/27/83

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 1 OF 8

COMMENTS	TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
19			1	1	1	1	3050-1007	RESISTOR	R45		1.0 Ω, ½W, 5%	
20			2	1	2	1	3050-3906		R25 [1] R57		39Ω, ½W, 5%	
21			1	1	1	1	3050-1000		R33		100Ω, ½W, 5%	
22			1	1	1	1	SELECTED AT TEST		R23		S.A.T.	
23			2	—	2	—	3000-2262		R67, 68		22K, ¼W, 5%	
24			1	1	1	1	3200-0008		R48		1.0 Ω, 1W, 3%	
25			1	1	1	1	3070-1501		R28		1.5 KΩ, 1W, 5%	
26			1	1	1	1	3100-7500		R13		75 Ω, ⅛W, 1%	
27			1	1	1	1	3100-6040		R14		604	
28			1	1	1	1	3100-8250		R15		825	
29			1	1	1	1	3100-9090	RESISTOR	R16		909 Ω, ⅛W, 1%	
30			1	1	1	1	3300-0084	RES. VAR.	R47		50K	
31			3	3	3	3	3300-0085		R20, 21, 32		100K	
32			1	1	1	1	3300-0088	RES. VAR.	R29		1MEG	
33			1	1	1	1	4100-0024	CAPACITOR	C43		68 PF, 500V MKA	
34			1	1	1	1	4100-0002		C39		470PF, 500V MICA	
35			8	6	8	6	4000-0009		C33, 35, 42, 44-46 [1] C5, 6,		0.1MF, 100V	
36			5	4	5	4	4400-0043	CAPACITOR	C1, C4, C24, C27 [1] C19		4.7MF, 6V	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
H	REV'D PER ECO NO 4562	6/8/84	JLL	DGW	JMS
J	PER ECO 4639	11/28/84	JLL	DGW	JMS

DASH NO.	NUMBER	QTY

NEXT ASSEMBLY

DRAWN M WOLFE DATE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 2 OF 8

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER D75AR

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
37			2	2	2	2	4000-0042	CAPACITOR	C36,49		.15uF, 100V	
38			—	—	—	1	4400-0039		C50		10uf / 16V	
39			3	3	3	3	4000-0043		C32,34,37		.01uF. 500V	
40			26	17	26	17	4010-0103		C40.41.2.3.8.9.13.14.16.21-23.25.26.28.29.48 [1] C7.12.17.18.20.54.57.58.59		.01uF, 50v	
41			1	—	1	—	4010-0100		C11		10pf, 100v	
42			1	1	1	1	4400-0036		C51		1000uF, 16V	
43			2	2	2	2	4400-0037		C47,54		470 uF, 25V	
44			1	1	1	—	4400-0047		C52		220uF, 35v	
45			1	1	1	1	4200-0036-10	CAPACITOR	C52		6uF, 200V	
46			1	1	1	1	4400-0038	CAPACITOR	C38		10uf, 100 V	
47			1	—	1	—	7000-0451	BATTERY	B1	POWER CONV INC.	2.4V NICD	
48			1	1	1	1	1200-0033	DIODE	CR5	35F4		
49			3	3	3	3	1200-0031	DIODE	CR3,4,6	IN4937		
50			1	1	1	1	4300-0041	CAPACITOR	C53		.056uf, 400V	
51			1	—	1	—	3000-3900	RESISTOR	R60		390Ω, 1/4W, 5%	X
52			3	1	3	1	6100-0151	SOCKET	X2E / [1] X1B, X3B		28 PIN	
53			1	1	1	1	SELECTED AT TEST	CAPACITOR	C30		S.A.T.	
54			1	—	1	—	4600-0010	CAP, VAR	C10		7-40 pf	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DRAWN M. WOLFE DATE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 3 OF 8

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER D75AR

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
55			2	1	2	1	1300-0028	TRANSISTOR	Q2 [1] Q6	2N3904		
56			1	—	1	—	1400-0019		Q1	2N3906		
57			1	1	1	1	1300-0049		Q5	BV407		
58			1	1	1	1	1300-0048	TRANSISTOR	Q4	2N4921		
59			2	2	2	3	6100-0120	SOCKET	X3,1 [1] X8B, X10B		16 PIN	
60			1	—	1	—	3000-6800	RESISTOR	R51		680Ω, 1/8W, 5%	
61			—	—	—	1	0950-0195	IC	10B		PROM, HORIZ	
62			8	8	8	8	3700-0083	RESISTOR PACK	RP15,6,9,12,15,20, [1] RP14 RP2		2.2K Ω, 10 PIN SIP	
63			5	—	5	—	3700-0085		RP 3,7,8,11,21		22K Ω 10 PIN SIP	
64			7	5	7	5	3700-0049	RESISTOR PACK	RP10,16-19 [1] RP4,13		3K/6.2K Ω 10 PIN SIP	
65			1	1	1	1	1500-0018	TRANSISTOR	Q3		VN10KM	
66			1	1	1	1	1800-0105	I.C.	7C	74LS00		
67			1	1	1	1	1800-0123		6C	74LS14		
68			2	1	2	1	-0110		9D [1] 5D	74LS10		
69			1	1	1	1	-0111		8D	74LS20		
70			2	1	2	1	-0117		7B [1] 17E	74LS74		
71			2	—	2	1	-0254		7E [1] 5E,6E	74LS85		
72			1	1	1	1	1800-0404	I. C.	9C	74LS136		

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DRAWN M. WOLFE DATE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 4 OF 8

PLAN HOLD CORPORATION • IRVINE CALIFORNIA

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
73			1	1	1	1	1800-0301	I.C.	14E	74LS156		
74			6	4	6	4	-0125		7A-10A [1] 15E,16E	74LS161		
75			1	1	1	1	-0121		9B	74LS175		
76			3	2	3	2	-0267		10D, 9E [1] 6B	74LS240		
77			3	2	3	2	-0240		13E, 9E [1] 5B, 1D	74LS244		
78			3	1	3	1	-0268		10E [1] 3C, 4C	74LS245		
79			3	—	3	1	-0231		12E [1] 3D 4D	74LS273		
80			1	1	1	1	-0193		8E	74LS138		
81			2	1	2	1	-0097		10C [1] 18E	7406		
82			1	1	1	1	1800-0038		8C	7452D		
83			1	—	1	—	0114-0064		8B		PROM, VERTICAL	
84			2	—	2	—	1820-0080		18,3B		IC/ST RAM CMOS	
85			1	1	1	1	1800-0319		2E	8259-A		
86			1	—	1	—	0114-0065		10B		PROM, HORIZONTAL	
87			1	1	1	1	1700-0082		11B	TDA-1270	VERTICAL PROCESSOR	
88			1	—	1	—	1800-0341		2D	MSM5832		
89			1	—	1	—	1800-0311	I.C.	7D	7438		
90			—	—	-	1	0950-0194	I.C.	8B		PROM, VERT	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M. WOLFE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 5 OF 8

PLAN HOLD CORPORATION • IRVINE CALIFORNIA

COMMENTS		TOTAL COST	UNIT COST

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
91			1	1	1	1	9000-0049	COIL ASSY, WTH	L1		5-30 UH	
92			1	1	1	1	0113-0011	COIL ASSY, LIN	L2			
93			1	—	1	—	5100-0018	CRYSTAL	Y1		32.768 KHZ	
94			1	1	1	1	0113-0014	TRANSFORMER	T1			
95			1	1	1	1	9000-0082	TRANSFORMER	T2		FLYBACK	
96			1	1	1	1	7000-0365	HEATSINK	@Q5			
97			1	1	1	1	7000-0366	HEATSINK	@11B			
98			1	1	1	1	7000-0221	INS. WASH	@Q5			
99			1	1	1	1	7200-0017	INSULATOR	@Q5			
100			1	1	1	1	2400-0004	MTG BRACKET	@T1			
101			1	1	1	1	6000-0359-6	HEADER	P1		6PIN	
102			1	1	1	1	6000-0359-8		P2		8PIN	
103			1	1	1	1	6000-0359-10	HEADER	P3		10PIN	
104			1	2	1	2	7000-0120	EJECTOR				
105			1	1	1	1	9000-0054	GND WIRE				
106			2	—	2	-	7200-0032	MOUSE TAIL			.115 DIA, 4"	
107			—	—	—	1	6600-0037	DIP SWITCH	S1			
108			2	2	2	2	3000-1001	RESISTOR	R10,69		1K, 1/4W, 5%	

ASSEMBLY TIME	COMPONENT LEAD SPACING

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN M. WOLFE 11/22/82
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 6 OF 8

PLAN HOLD CORPORATION • IRVINE CALIFORNIA

COMMENTS	TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF DESIGNATION	VENDOR NO	DESCRIPTION	TYPE
109			1	1	1	1	3000-2200	RESISTOR	R26		220Ω, ¼W, 5%	
110			1	1	1	1	3000-3300	RESISTOR	R27		330Ω, ¼W, 5%	
111			1	—	1	—	3300-0096	RES., VAR	R56		1K, 1 TURN	
112			1	—	1	—	7400-0002	BEEPER				
113			1	—	1	—	1700-0071	I.C.	11C		LF356	
114			1	—	1	—	4400-0045	CAPACITOR	C55		33μf, 25v	
115			1	—	1	—	0112-0228-08	EJECTOR, STAMPED			"A8"	
116			1	—	1	—	1800-0351	I.C.	5C		74LS12	
117			1	—	1	—	1800-0352	I.C.	6D		74LS22	
118			1	—	1	—	3000-5106	RESISTOR	R61		51Ω, ¼W 5%	X
119			1	—	1	—	1000-0002	DIODE	CR7		1N4152	X
120			0.1	—	0.1	—	8300-0027	INSULATION	3M4108		1"x 1"x 1/8"THK	
121			1	—	1	—	4000-0011	CAPACITOR	C61		2.2 mf	
122			1	—	1	—	6000-0389	HEADER	P4		34 PIN - FLOPPY	
123			1	—	1	—	6100-0146	SOCKET	2D		18 PIN	
124												
125			1	—	1	—	3000-2700	RESISTOR	R7		270Ω, ¼W, 5%	
126			1	—	1	—	3000-3301	RESISTOR	R50		3.3K ¼W. 5%	

REF DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

DRAWN M. WOLFE 11/22/83
CHECKED
ENGINEER
MANUFACTURING
QUALITY ASSURANCE

LIST OF MATERIAL
DATA DISPLAY
PWB ASSY

biomation

B | 0114-2010 | REV J

MODEL K101/K500 | CODE | SHEET 7 OF 8

PLAN HOLD CORPORATION • IRVINE CALIFORNIA

ITEM	QUANTITY PER ASSEMBLY -60	-50	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
127						1	—	1	—	0114-0432	LABEL, CAUTION NICD ONLY!		I
128						2	2	—	—	7011-1440-10	SCREW 4-40X5/16 PH		X
129						1	1	—	—	0117-0149-10	PROM, VERT, K105	8B	
130						1	1	—	—	0117-0150-10	PROM, HORIZ, K105	10B	
131													
132						1	1	—	—	0117-0139-10	SHIELD, DEFLECTION		X
133						2	2	-	-	7084-1004-00	#4 STAR WASHER		X
134						2	2	-	-	7080-1004-00	#4 SMALL WASHER		X
135						—	—	REF	—	30 AWG KYNAR	JUMPER WIRE	PIN 19 2D (REF. SHT 6 SCHEM.)	
136						1.3	1.3	1.3	1.3	7150-0018-09	WIRE 19 STRAND WHITE	SEE NOTE 5	

NOTES

LIST OF MATERIAL
DATA DISPLAY PWA ASSY

GOULD → biomation

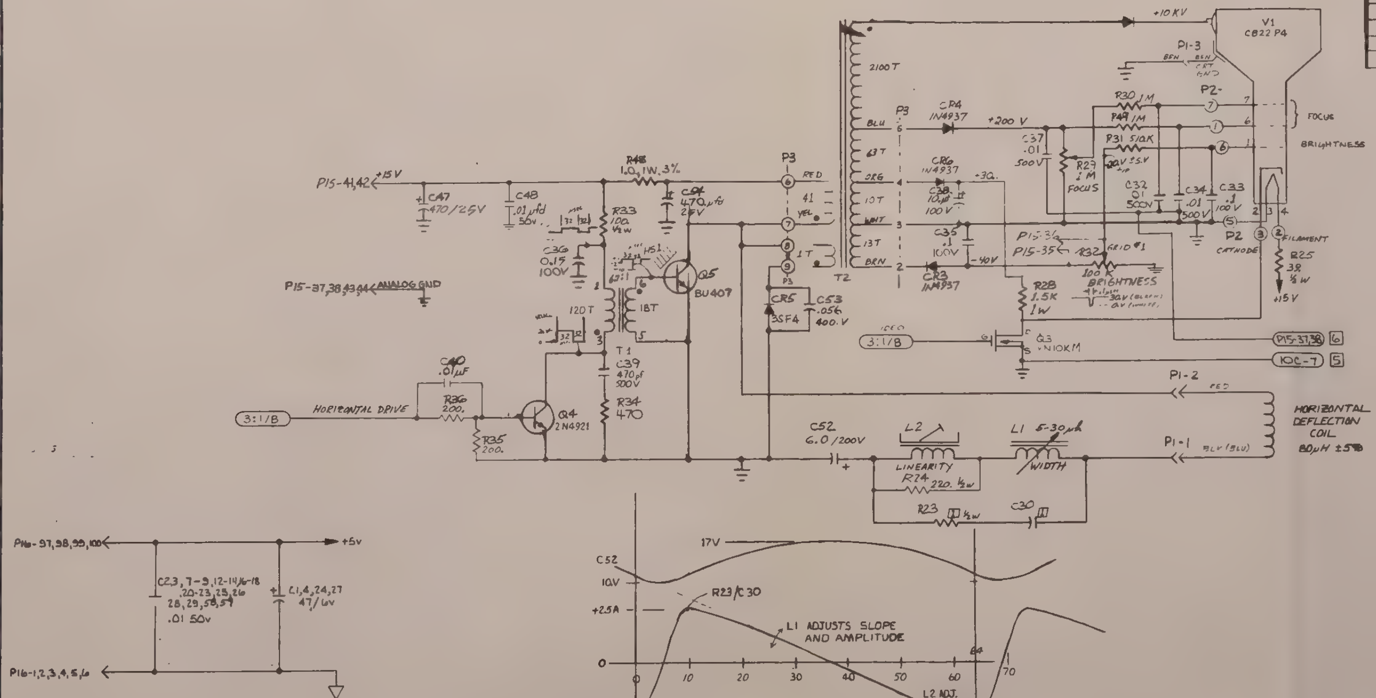
B | 0114-2010 | REV J

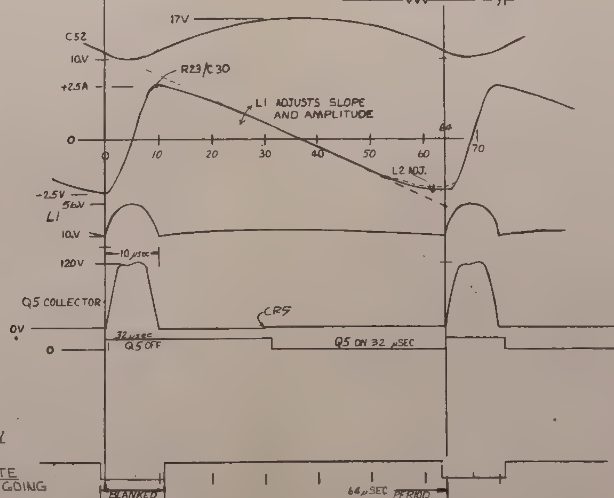
MODEL K101/K500 | SHEET 8 OF 8

KLINGLER MFG. H 10

DWG NO 0114-20 SH 1 REV J

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	A		PRODUCTION RELEASE ERN#295			
	B		PRODUCTION RELEASE ERN#302			
	C		REV'D PER ECO	MW	DCW	[illegible]
	D	3865	REVISED PER ECO	MW	DCW	[illegible]
	E	3906	REVISED PER ECO	MW	DCW	[illegible]
	F	4147	REVISED PER ECO	MW	[illegible]	[illegible]
	G	4463	REVISED PER ECO	JG	[illegible]	[illegible]
	H	4562	REVISED PER ECO NO	JWC	[illegible]	[illegible]
	J	4629	PER ECO	[illegible]	[illegible]	[illegible]





NOTES: UNLESS OTHERWISE SPECIFIED

1. SELECTED AT TEST. NOT NORMALLY USED. R23 = 100Ω C30 = .002µf MAY BE USED TO GIVE A SMALL CORRECTION OF HORIZ LINEARITY AT LEFT SIDE OF DISPLAY
2. ALL RESISTOR VALUES ARE IN OHMS. 1/4W, ±5%
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. -10 ONLY
5. Q3 SOURCE MUST HAVE A SEPERATE WIRE OR TRACE EQUIVALENT TO 18AWG 19 STRAND WIRE GOING DIRECTLY TO 10C-7.
6. THE GROUNDED SIDES OF C32 C34 & C37 MUST HAVE A SEPERATE WIRE OR TRACE EQUIVALENT TO 18 AWG 19 STRAND WIRE GOING DIRECTLY TO P15-37,38.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			✓	✓				1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DASH NO | NUMBER | QTY — NEXT ASSEMBLY

ENG. SERV | DATE

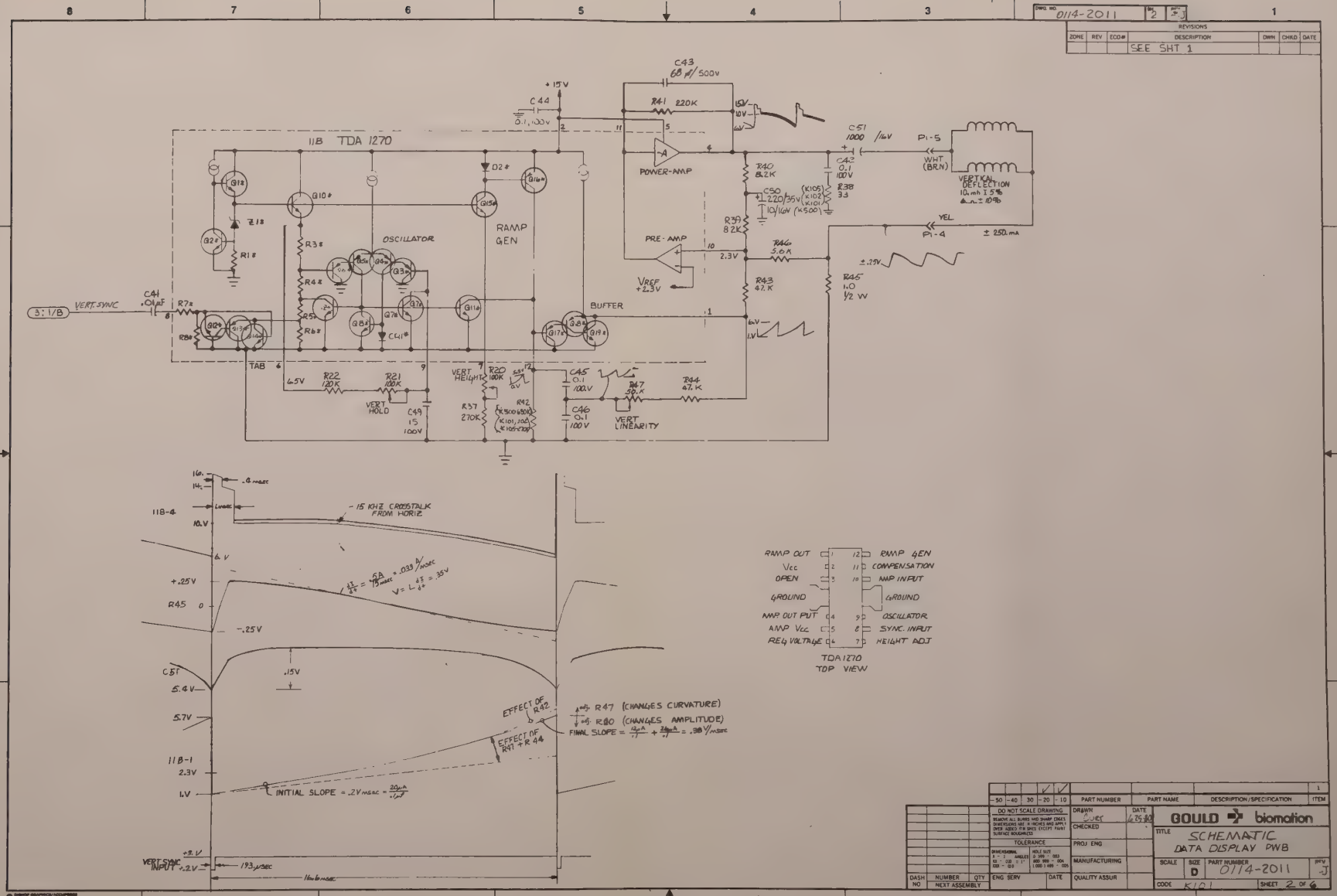
DRAWN: CURT — 6-25-80
CHECKED: [illegible] — 12/9/82
PROJ. ENG.: Curt — 1/26/83
MANUFACTURING
QUALITY ASSUR: [illegible] — 1/27/83

GOULD biomation

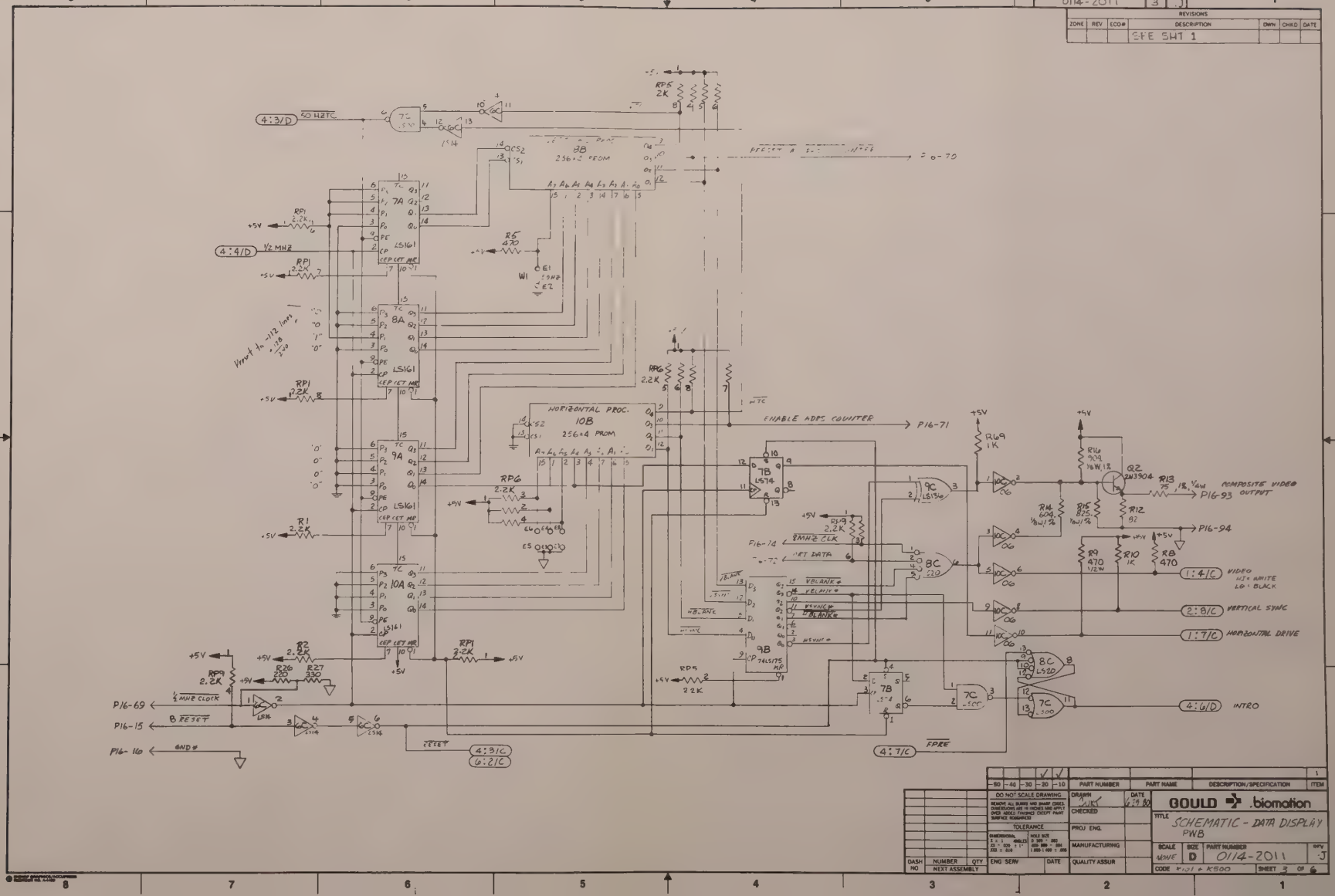
TITLE: SCHEMATIC DATA DISPLAY PWB

SCALE | SIZE D | PART NUMBER 0114-2011 | REV J

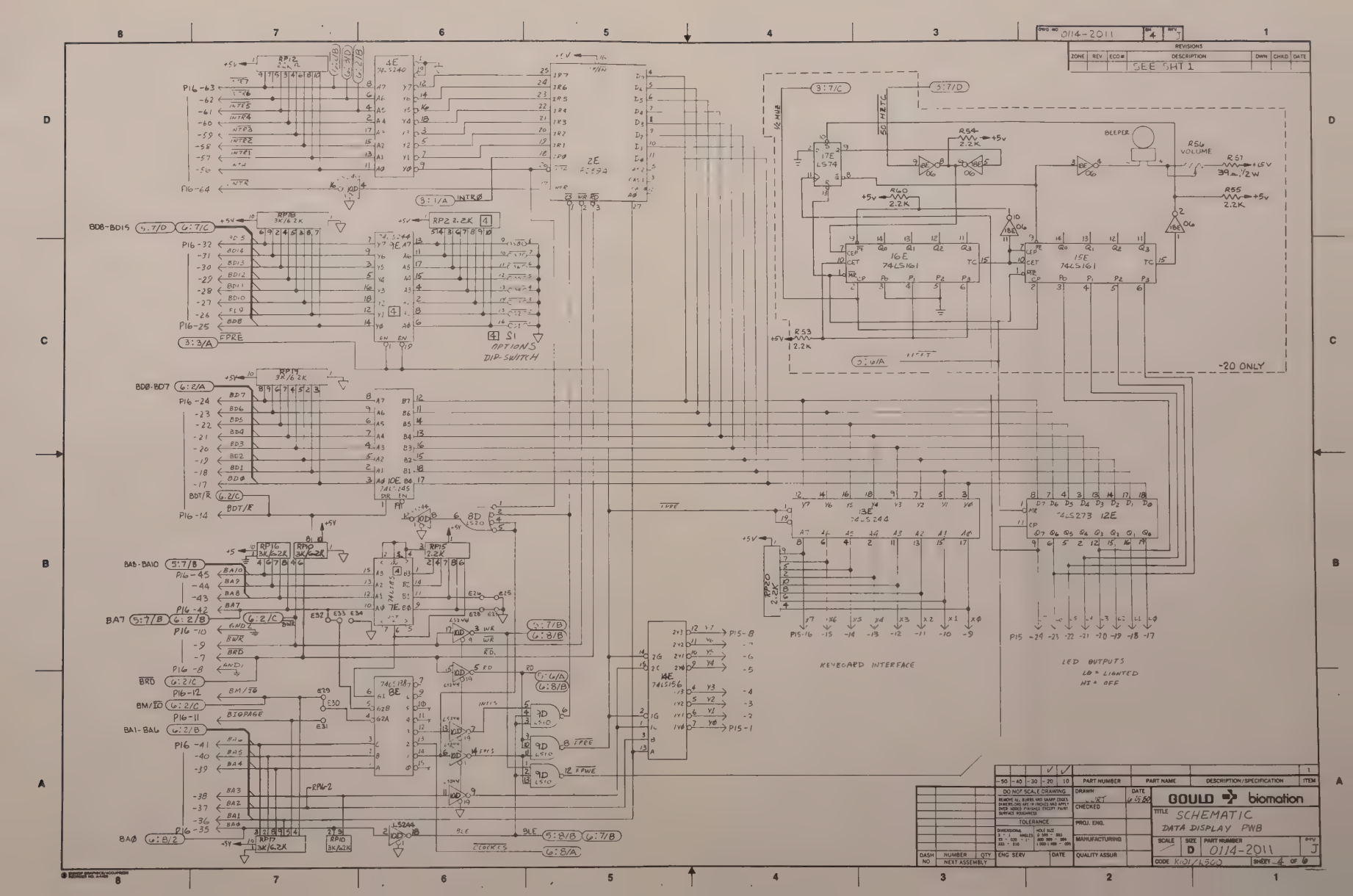
CODE K101 + K500 | SHEET 1 OF 6

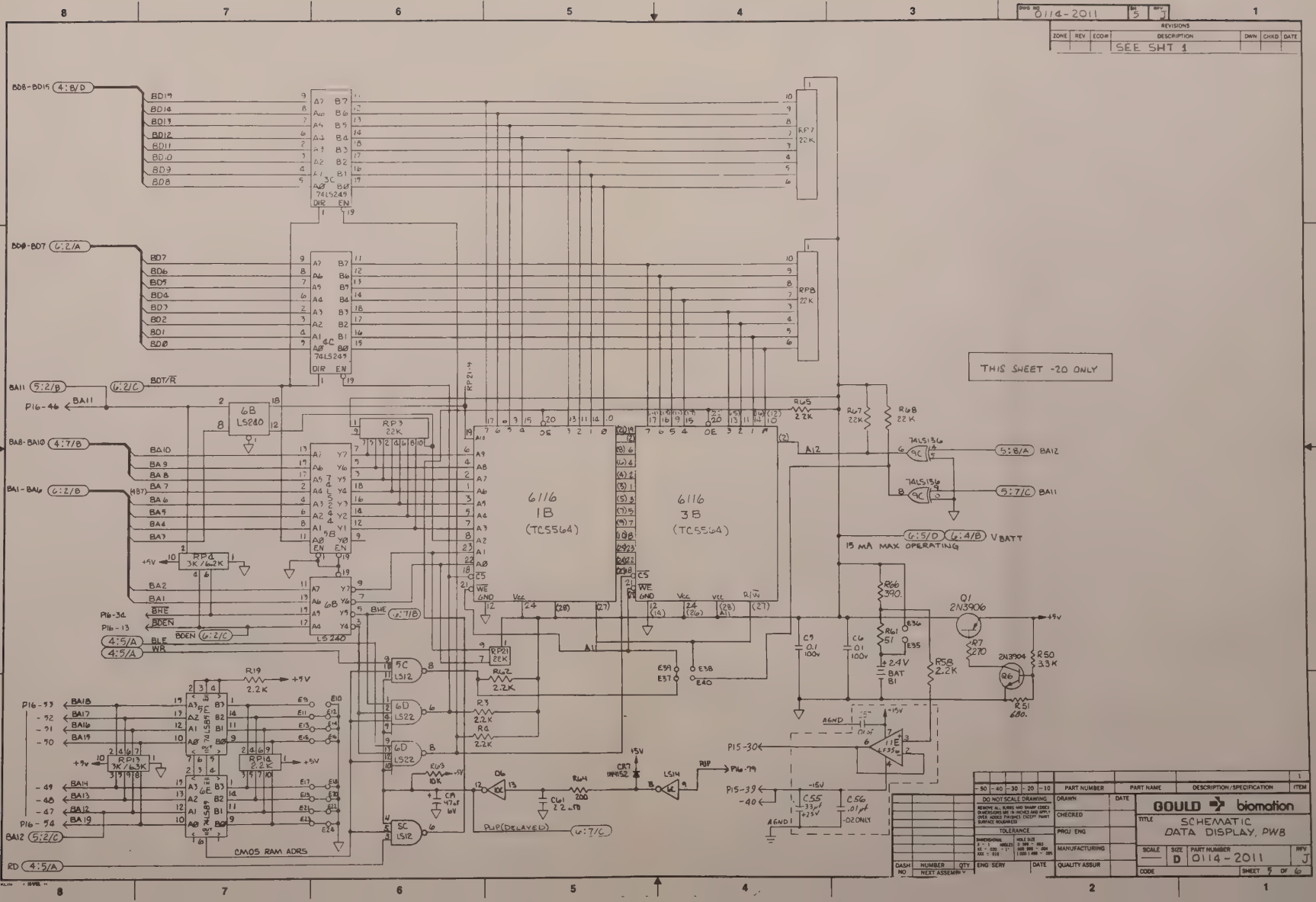


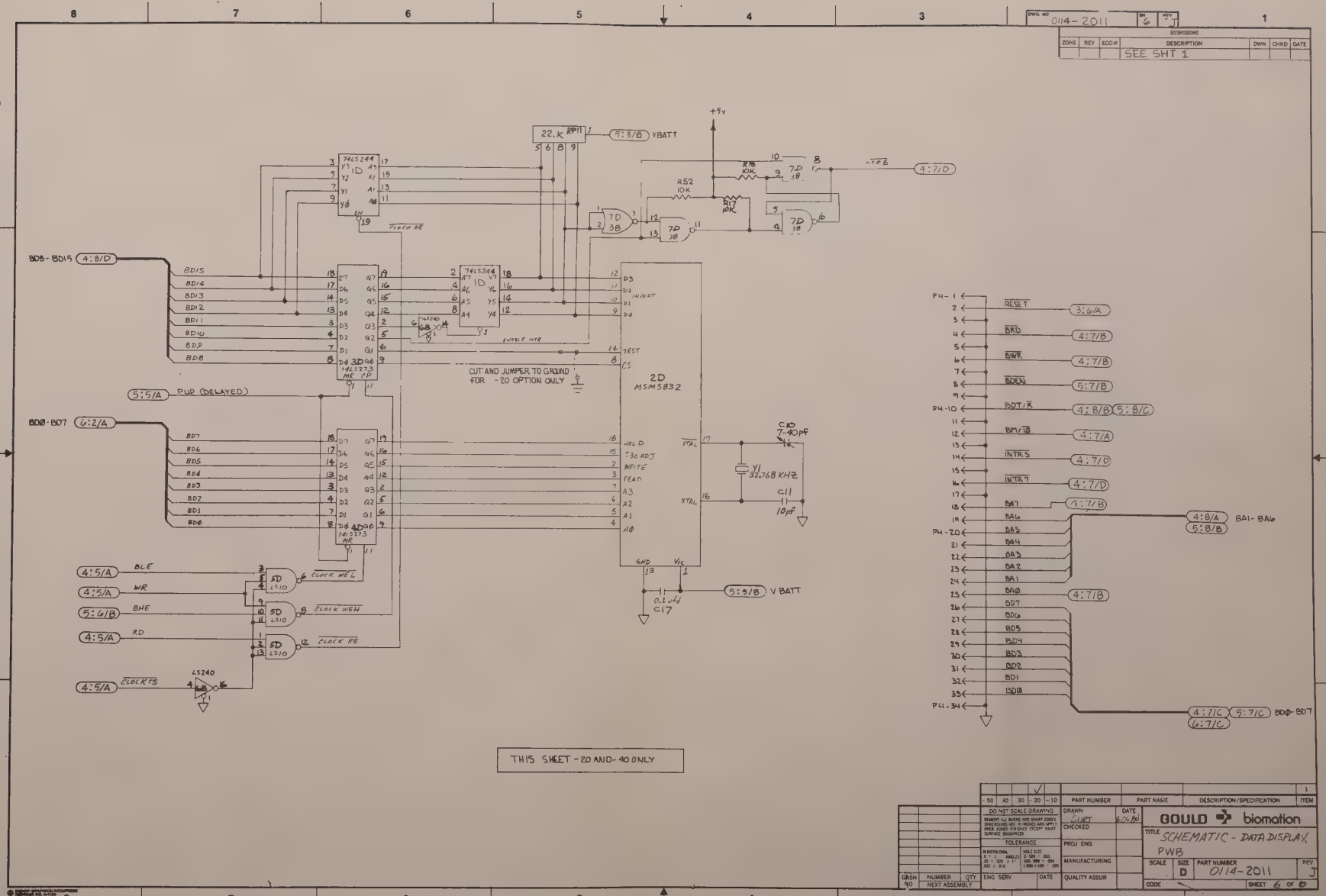
DWG. NO. 0114-2011
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
C43 68 pf/500v
+15V
C44 0.1, 100v
R41 220K
11B TDA 1270
POWER-AMP
PRE-AMP
VREF +2.3V
OSCILLATOR
RAMP GEN
BUFFER
TAB
C51 1000 /16V
P1-5
WHT (BRN)
VERTICAL DEFLECTION 10.mh I 5% ± 10%
YEL
P1-4
± 250.mA
R40 8.2K
C42 0.1 100V
C50 220/35V 10/16V
R38 33
R39 8.2K
R46 5.6K
R43 47.K
R45 1.0 1/2 W
3:1/B VERT. SYNC
C41 .01µF
R7
R8
R22 120K
R21 100K
VERT HOLD
C49 15 100V
VERT HEIGHT
R20 100K
R37 270K
R42
C45 0.1 100V
C46 0.1 100V
R47 50.K
R44 47.K
VERT LINEARITY
11B-4
-15 KHZ CROSSTALK FROM HORIZ
R45
C51
EFFECT OF R42
EFFECT OF R47 + R44
R47 (CHANGES CURVATURE)
R80 (CHANGES AMPLITUDE)
FINAL SLOPE = 12µA/.1 + 24µA/.1 = .38V/msec
11B-1
INITIAL SLOPE = .2V msec = 20µA/.1µF
VERT SYNC INPUT
193 µsec
16.6 msec
RAMP OUT
Vcc
OPEN
GROUND
AMP OUT PUT
AMP Vcc
REG VOLTAGE
RAMP GEN
COMPENSATION
AMP INPUT
GROUND
OSCILLATOR
SYNC. INPUT
HEIGHT ADJ
TDA1270 TOP VIEW
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
GOULD biomation
TITLE SCHEMATIC DATA DISPLAY PWB
SCALE
SIZE D
PART NUMBER 0114-2011
REV J
CODE K101
SHEET 2 OF 6
DASH NO
NUMBER
QTY
NEXT ASSEMBLY



DWG. NO. 0114-2011
SH 3
REV J
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SEE SHT 1
4:3/D
50 HZTC
4:4/D
1/2 MHZ
7A
8A
9A
10A
LS161
8B
256x4 PROM
HORIZONTAL PROC.
10B
256x4 PROM
ENABLE ADRS COUNTER
P16-71
7B
LS74
9C
LS136
8C
LS20
9B
74LS175
7C
LS00
COMPOSITE VIDEO OUTPUT
P16-93
P16-94
1:4/C
VIDEO
HI = WHITE
LO = BLACK
2:8/C
VERTICAL SYNC
1:7/C
HORIZONTAL DRIVE
4:6/D
INTRO
4:7/C
FPRE
4:3/C
6:2/C
RESET
P16-69
1/2 MHZ CLOCK
P16-15
B RESET
P16-16
GND#
Vrest to -112 lines
DO NOT SCALE DRAWING
TOLERANCE
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DRAWN
DATE
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE
SCHEMATIC - DATA DISPLAY PWB
SCALE
NONE
SIZE
D
PART NUMBER
0114-2011
REV J
CODE K101 + K500
SHEET 3 OF 6


DWG NO 0114-2011
REV J
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
4E 74LS240
2E 2732
3E 74LS240
5E 74LS273
12E
13E 74LS244
16E 74LS161
15E 74LS161
17E LS74
KAE 74LS156
BE 74LS138
RP12 2.2K
RP13 3K/6.2K
RP14 3K/6.2K
RP15 2.2K
RP16 3K/6.2K
RP17 3K/6.2K
RP18 3K/6.2K
RP19 3K/6.2K
RP20 2.2K
RP2 2.2K
R53 2.2K
R54 2.2K
R55 2.2K
R56 VOLUME
R51 39Ω 1/2W
R40 2.2K
BEEPER
S1 OPTIONS DIP-SWITCH
-20 ONLY
KEYBOARD INTERFACE
LED OUTPUTS
LO = LIGHTED
HI = OFF
BD8-BD15
BD0-BD7
BA8-BA10
BA0-BA7
INTR8
EPRE
BDTR
BWR
BRD
BM/IO
BIOPAGE
TPEE
TPWE
BLE
CLOCK65
BOULD biomation
TITLE SCHEMATIC
DATA DISPLAY PWB
SCALE / SIZE D PART NUMBER 0114-2011 REV J
CODE K1001/1342 SHEET 4 OF 6
DRAWN WKT 6/15/82
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG SERV
DO NOT SCALE DRAWING
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DASH NO
NUMBER NEXT ASSEMBLY
QTY


DWG NO 0114-2011 SH 5 REV J
REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
SEE SHT 1
THIS SHEET -20 ONLY
6116 1B (TC5564)
6116 3B (TC5564)
74LS245
74LS240
74LS139
74LS136
74LS32
74LS14
74LS12
74LS85
15 MA MAX OPERATING
VBATT
CMOS RAM ADRS
PUP(DELAYED)
GOULD biomation
SCHEMATIC
DATA DISPLAY, PWB
SCALE —
SIZE D
PART NUMBER 0114-2011
REV J
SHEET 5 OF 6

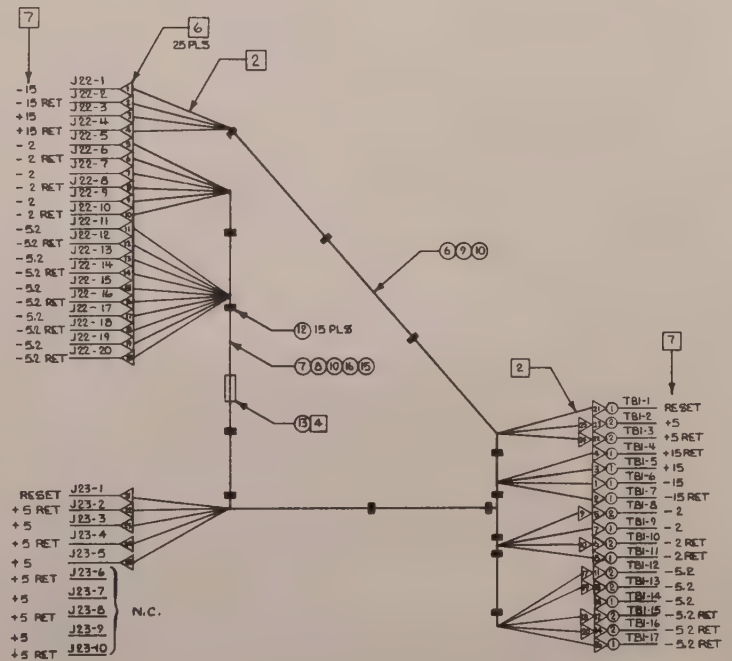


DWG. NO 0114-2011
SH 6
REV J
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
SEE SHT 1
22.K RP11
5:3/B VBATT
+5V
R52 10K
R18 10K
R17 10K
7D 38
4:7/D
74LS244 1D
74LS273 MR
BD8-BD15 4:8/D
BD0-BD7 6:2/A
5:5/A PUP (DELAYED)
CLOCK RE
ENABLE INTR
CUT AND JUMPER TO GROUND FOR -20 OPTION ONLY
2D MSM5832
HOLD
±30 ADJ
WRITE
READ
GND
Vcc
XTAL
C10 7-40pf
Y1 32.768 KHZ
C11 10pf
C17 0.1 ufd
5:3/B V BATT
4:5/A BLE
4:5/A WR
5:6/B BHE
4:5/A RD
4:5/A CLOCK CS
LS240
5D LS10
CLOCK WEL
CLOCK WEH
CLOCK RE
P4-1
RESET 3:6/A
BRD 4:7/B
BWR 4:7/B
BDEN 5:7/B
P4-10
BDT/R 4:8/B 5:8/C
BM/IO 4:7/A
INTR5 4:7/D
INTR7 4:7/D
BA7 4:7/B
BA6
P4-20
BA5
BA4
BA3
BA2
BA1
BA0 4:7/B
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
P4-34
4:8/A 5:8/B BA1-BA6
4:7/C 5:7/C 6:7/C BD0-BD7
THIS SHEET -20 AND -40 ONLY
-50 40 30 -20 -10
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
ENG SERV
DATE
GOULD biomation
TITLE SCHEMATIC - DATA DISPLAY, PWB
SCALE
SIZE D
PART NUMBER 0114-2011
REV J
CODE
SHEET 6 OF 6
DASH NO
NUMBER
QTY
NEXT ASSEMBLY

DWG NO	SH	REV
0114-2024	1	D

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DATE	CHKD	APPD
	C	4549	PER ECO		GG	
	D	4723	REDRAWN	9-10-84	JWC	



WIRE NO	FROM	TO	AWG	LNG ±.25	COLOR
1	J22-1	TB1-6	16	13.5	VIO
2	J22-2	TB1-7	16		BLK
3	J22-3	TB1-5	16		ORN
4	J22-4	TB1-4	16	13.5	BLK
5	J22-5	TB1-8	16	16.5	GRY
6	J22-10	TB1-10	16		BLK
7	J22-7	TB1-9	16		GRY
8	J22-8	TB1-11	16		BLK
9	J22-9	TB1-8	16		GRY
10	J22-10	TB1-10	16		BLK
11	J22-11	TB1-12	16		VIO
12	J22-12	TB1-15	16		BLK
13	J22-13	TB1-13	16		VIO
14	J22-14	TB1-16	16		BLK
15	J22-15	TB1-14	16		VIO
16	J22-16	TB1-17	16		BLK
17	J22-17	TB1-12	16		VIO
18	J22-18	TB1-15	16		BLK
19	J22-19	TB1-13	16		VIO
20	J22-20	TB1-16	16	16.5	BLK
21	J23-1	TB1-1	16	12.5	YEL
22	J23-2	TB1-3	16		BLK
23	J23-3	TB1-2	16		GRY
24	J23-4	TB1-3	16		BLK
25	J23-5	TB1-2	16	12.5	GRY

7

-15
-15 RET
+15
+15 RET
-2
-2 RET
-2
-2 RET
-5.2
-5.2 RET
-5.2
-5.2 RET
RESET
+5 RET
+5
+5 RET
+5

NOTES: UNLESS OTHERWISE SPECIFIED

1. DRAWING IS TO SCALE AND MAY BE USED AS A TEMPLATE.
2. IDENTIFY LUGS AND ENDS OF WIRES WITH DESTINATION AS SHOWN.
3. TIP OF TERMINATION TRIANGLE DENOTES END OF CUT WIRE BEFORE LUGGING.
4. TAG HARNESS WITH ASSY NO., DASH NO., AND REV. LEVEL.
5. ▽ TERMINATION TRIANGLE INDICATES WIRE NO.
   ○ CIRCLE INDICATES ITEM NO. ON PARTS LIST.
6. ENDS OF WIRES STRIPPED AND TINNED 1/4"
7. SIGNAL NAMES SHOW FOR REF. ONLY.
8. N.C. MEANS "NO CONNECTION."

-03 QTY PER ASSY	-02 QTY PER ASSY	-01 QTY PER ASSY	PART NUMBER	DESCRIPTION	ITEM NO
10	10	10	0950-0220	K500	
10	10	10	0120-0080	K205	
10	10	10	0114-0210	K101	

PARTS LIST

DASH NO	NEXT ASSY	USED ON
FIRST APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

MATERIAL

FINISH

GOULD PART NO.

APPROVALS	DATE
DRAWN J.W. CARROLL	9-10-84
CHECKED D.G.W.	6-4-84
PROJ ENG J.S.	6-15-84

GOULD Electronics

TITLE: CABLE ASSEMBLY POWER SUPPLY

SIZE D | DWG NO 0114-2024 | REV D.

SCALE 1/1 | MODEL | SHEET 1 OF 1

GOULD

TITLE	LM	DRAWING NO.	REV
ASSEMBLY CABLE, POWER SUPPLY		0114-2024	D

DWN	CHK	ENG	MFG	MODEL	SHEET / OF /
JWC	DGW			K101	

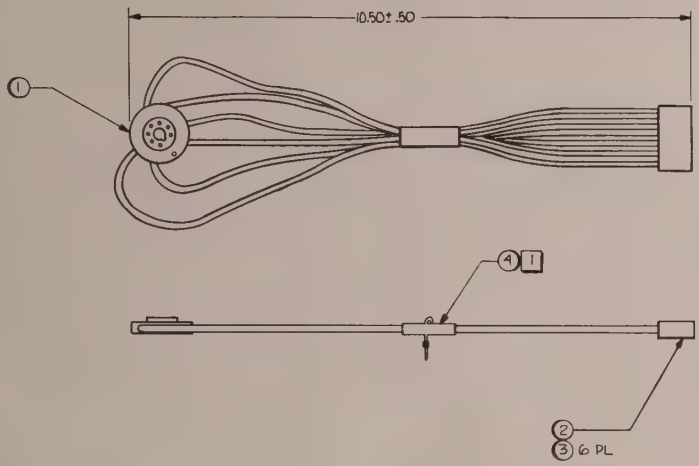
ITEM NO.	PART NUMBER	QTY PER ASSY -10	-20	-30	-40	-50	U/M	DESCRIPTION	REFERENCE DESIGNATION
1	6200-0069-10	9						LUG, FORK 18-22	
2	6200-0055-10	8						LUG, FORK 10-12, #6	
3									
4									
5	7150-0016-08	6.5FT						WIRE, 16 AWG GRY	
6	-03	1.1FT						ORN	
7									
8									
9	-07	7.9FT						VIO	
10	7150-0016-10	15.5 FT						WIRE 16 AWG BLK	
11									
12	7200-0008-10	15						CABLE TIE	
13	7200-0039-10	1						MARKER TIE	
14									
15	7150-0016-04	1.2FT						WIRE, 16 AWG, YEL	
16									

REV	ECO	CHK	APPD	DATE
A	3886	DGW		9-21-83
B	4305	TK	JMS	3/6/84
C	4549	DGW	JMS	6/12/84
D	4723	DGW		10/5/84

NOTES:

DASH#	NEXT ASSY	QTY
-10	0114-0210	1
-10	0120-0080	1
-10	0950-0220	1

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 309	STM	[illegible]	2/4/83
	A	3957	PROD REL PER ECO # [illegible]	STM	[illegible]	9/16/83



WIRING CODE	
PIN	COLOR
1	ORG
2	BRN
3	VIO
4	N/C
5	BLK
6	GRN
7	BLU
8	N/C

1 MARK PART WITH PART NO. 0117-0021 DASH NO. & REV LEVEL USING 1/8" CHARACTERS.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO	NUMBER	QTY
10	0117-0123	1
	NEXT ASSEMBLY	

ENG SERV R [illegible] DATE 2/3/83

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY AFTER ADDED FINISHES (EXCEPT PAINT). SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: ± .020 .1° .014 — ANGLES: ± 1° — HOLE SIZE: 0.1-0.99 .002, 1.00-7.99 .004, OVR .004

DRAWN STM DATE 12-1-82

CHECKED

SHIPPING ENG [illegible] 2/3/83

MANUFACTURING [illegible] 2-3-83

QUALITY ASSUR [illegible] 2-3-83

GOULD biomation

TITLE CRT CABLE ASSEMBLY

SCALE	SIZE	PART NUMBER	REV
NONE	C	0117-0021	A

CODE K105 SHEET 1 OF 1

KLINGLER H-10

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	6100-0130-10	SOCKET, CRT		
2									1	6000-0358-08	HOUSING, 20 PIN		
3									6	6000-0357-10	PIN		
4									1	7200-0039-10	MARKER, TIE WRAP		
5													

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL PER ECO 3957	9-16-83	STM	[illegible]
50	PILOT REL PER ERN 309	2/4/83	STM	[illegible]

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-0123	1

DWN STM DATE 12-2-82

CHK

ENGR [illegible] 2/3/83

MFG. [illegible] 2-3-83

Q.A. [illegible] 2-3-83

LIST OF MATERIAL
CRT CABLE ASSEMBLY

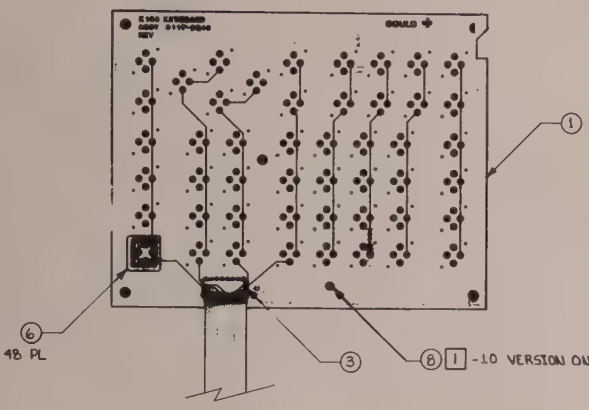
GOULD biomation

B 0117-0021 REV A

MODEL K105 SHEET 1 OF 1

KLINGLER H-10

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 316	SJN		2-3-83
	51	3695	REV'D PER ECO #	MW	DLW	4/6/83
	52	3739	REV'D PER ECO #	MW	DLW	5/8/83
	A	3957	PROD REL PER ECO	[illegible]	DLW	7/6/83
	B	4220	PER ECO	KR	DLW	1/17/84



1 FLAT SIDE (CATHODE) OF ITEM 8 GOES TO SQUARE PAD ON CIRCUIT BOARD, -10 VERSION ONLY.

NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: 2 ± 1 ANGLES; .XX ± .020 ± 1°; .XXX ± .010
HOLE SIZE: 0 .199 ± .001; .200 .199 ± .004; 1 .000 1 .000 .005

DASH NO	NUMBER	QTY
-20	0120-0008	1
-10	0117-0008	1

NEXT ASSEMBLY

ENG SERV: R Sagan — DATE: 2/18/83

DRAWN: J.W. CARROLL — DATE: 6-4-82
CHECKED: R Wood — 2/10/83
PROJ ENG: [signature] — 2-15-83
MANUFACTURING: [signature] — 2-16-83
QUALITY ASSUR

GOULD biomation

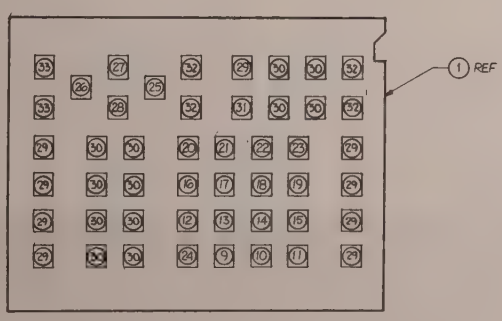
TITLE: ASSY -KEYBOARD

SCALE: 1:1 | SIZE: C | PART NUMBER: 0117-0040 | REV: B

CODE: K105 | SHEET 1 OF 2

0117-0040 1 B

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SH.1			



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: 2 ± 1 ANGLES; .XX ± .020 ± 1°; .XXX ± .010
HOLE SIZE: 0 .199 ± .001; .200 .199 ± .004; 1 .000 1 .000 .005

DASH NO | NUMBER | QTY
NEXT ASSEMBLY

ENG SERV: R Sagan — DATE: 2/18/83

DRAWN: [signature] — DATE: 12-7-82
CHECKED: R Wood — 2-15-83
PROJ ENG: [signature] — 2-18-83
MANUFACTURING: [signature] — 2-16-83
QUALITY ASSUR

GOULD biomation

TITLE: ASSEMBLY KEYBOARD

SCALE | SIZE: C | PART NUMBER: 0117-0040 | REV: B

CODE: K105 | SHEET 2 OF 2

0117-0040 2 B

ITEM	-90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1								1	1	0117-0042-10	K105 KEYBOARD PWB		
2													
3								1	1	0112-0204-10	CABLE ASSY KEY BD TO FRONT PANEL		L/M
4													
5													
6								48	48	6600-0118-10	SWITCH		
7													
8								—	1	6400-0039-10	L.E.D. RED	C.R.1.	
9								1	1	0112-0079-01	KEY TOP, WHITE	"1"	
10								1	1	-02		"2"	
11								1	1	-03		"3"	
12								1	1	-04		"4"	
13								1	1	-05		"5"	
14								1	1	-06		"6"	
15								1	1	-07		"7"	
16								1	1	-08		"8"	
17								1	1	-09		"9"	
18								1	1	-10		"A"	
19								1	1	-11		"B"	
20								1	1	-12		"C"	
21								1	1	-13		"D"	
22								1	1	-14		"E"	
23								1	1	-15		"F"	
24								1	1	0112-0079-16		"0"	
25								1	1	0112-0059-23	BLUE	"►"	
26								1	1	0112-0059-24		"◄"	
27								1	1	0112-0059-25	KEY TOP, BLUE	"▲"	

REV	DESCRIPTION	DATE	DWN	CKD
B	PER ECO 4220	1.17.83	Kaua	DGW JWS
A	PROD REL PER 3957	7/1/83		DGW
52	REV'D PER ECO # 3739	4/15/83	STM	DGW
51	REV'D PER ECO #3695	4/5/83	MW	DGW
50	PILOT REL PER ERN 316	2.5.83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
-20	0120-0008	1
-10	0117-0008	1

		DATE
DWN	J.W.CARROLL	6-4-82
CHK	R. Wood	2-15-83
ENGR	[signature]	2-18-83
MFG	[signature]	2-18-83
Q.A.		

LIST OF MATERIAL
ASSEMBLY -KEYBOARD

GOULD biomation
B 0117-0040 REV B
MODEL K105 SHEET 1 OF 2

KLINGLER K-VEL H-10

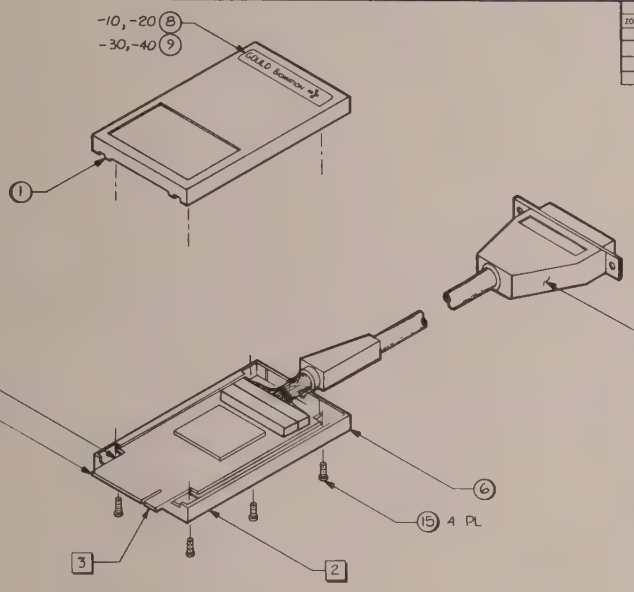
ITEM	-90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28								1	1	0112-0059-26	KEY TOP BLUE	"▼"	
29								9	9	-0049-10	BLUE PLAIN		
30								12	12	-0049-20	BLACK PLAIN		
31								1	1	0112-0049-50	KEY TOP RED PLAIN		
32								4	4	0112-0049-40	KEY TOP GREY PLAIN		
33								2	2	0112-0049-30	KEY TOP WHITE PLAIN		

NOTES

LIST OF MATERIAL
ASSY. KEYBOARD

GOULD biomation
B 0117-0040 REV B
MODEL K105 SHEET 2 OF 2

KLINGLER K-VEL H-10



REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE	STM		1-8-83
	50		PILOT REL PER ERN 335	STM		4-18-83
	51	3760	REVISED PER E.C.O.N°	JWC	[illegible]	8-29-83
	52	3749	REV'D PER ECO 3749	RTM	[illegible]	11-4-83

USAGE CHART		
DASH	MODEL	LENGTH
10	K105	6'
20	K105	9'
30	K101	6'
40	K101	9'

3 MARK BOTTOM OF CASE LARGE RECTANGULAR RECESS WITH THE FOLLOWING: XXX, XX, XX, XXXX
MFG N° YEAR WEEK SERIAL N°
0117-0099-XX REV A
DASH CURRENT REV LEVEL

2 BAG AND TAG WITH P/N 0117-0099, DASH NO. AND REV. LEVEL.

1 PIN 1 (FARSIDE).

NOTES: UNLESS OTHERWISE SPECIFIED

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
					DO NOT SCALE DRAWING	DRAWN STM	DATE 1-8-83	GOULD biomation
					REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY AFTER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS	CHECKED [illegible]	4/19/83	TITLE PROBE SUB ASSY
40	0114-1092					PROG ENG [illegible]	[illegible]	
40	0114-1091				TOLERANCE	MFG ENG [illegible]	[illegible]	
30	0114-1062				DIMENSIONAL HOLE SIZE	QUALITY/TESTING [illegible]	#13+3	SCALE NONE SIZE C PART NUMBER 0117-0099 REV 52
30	0114-1061				ANGLES ± .5° .XX ± .010 .XXX ± .005	QUALITY ASSUR [illegible]	9/14/83	CODE K105/K101 SHEET 1 OF 1
20	0117-0174				.13 .020 1/64 .500 TO .999 .004			
10	0117-0173				1/32 .030 .1000 TO 1.499 .005			
DASH NO	NUMBER NEXT ASSEMBLY		QTY		ENG. SERV R. Rogers	DATE 9/16/83		

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1						1	1	1	1	0114-0255-10	CASE, PROBE, TOP		
2						/	/	1	1	0117-0213-10	PROBE PWB ASSY, K105		
3						1	1	/	/	0117-0213-20	PROBE PWB ASSY, K101/K102		
4						/	1	/	1	0117-0022-10	POD TO UNIT CABLE 6'		
5						1	/	1	/	0117-0022-20	POD TO UNIT CABLE 9'		
6						1	1	1	1	0114-0255-20	CASE, PROBE, BOTTOM		
7													
8						/	/	1	1	0117-0171-10	LABEL, PROBE POD, K105		
9						1	1	/	/	0114-0264-10	LABEL, PROBE POD, K101/K102		
10													
11													
12													
13													
14													
15						4	4	4	4	7000-0429-20	SCREW 2 x 3/8" LG PH. HD.		

REV	DESCRIPTION	DATE	DWN	CKD
52	REV'D PER ECO 3749	11-4-83	RTM	[illegible] STM
51	REVISED PER ECO 3760	8-29-83	JWC	[illegible]
50	PILOT REL PER ERN 335	4-18-83	STM	
01	PROTOTYPE	1-8-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
40	0114-1092	1
40	0114-1091	1
30	0114-1062	1
30	0114-1061	1
20	0117-0174	1
10	0117-0173	1

DWN	STM	1-8-83
CHK	R. Wood	4/19/83
ENGR	[illegible]	7/6/83
MFG	[illegible]	8/25/83
QA	[illegible]	9/14/83

LIST OF MATERIAL

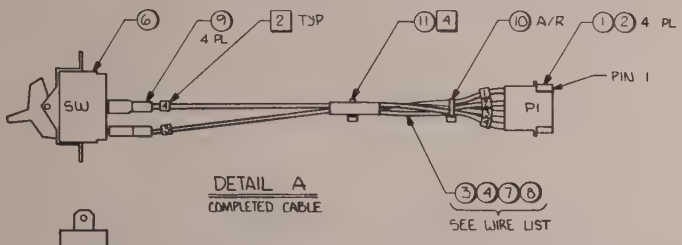
PROBE SUB ASSEMBLY

GOULD biomation

B 0117-0099 REV 52

MODEL K105-K101 SHEET 1 OF 1

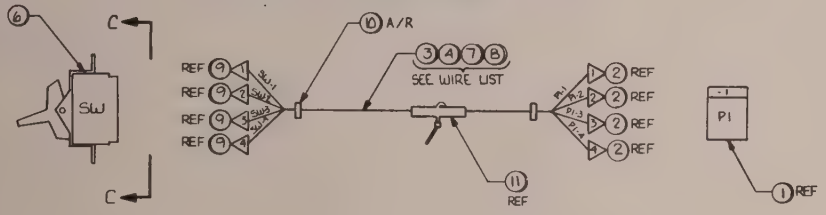
REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 316	STM		1-31-83
	A	3957	PROD REL PER ECO#	STM	DGW	7-16-83



DETAIL A
COMPLETED CABLE

VIEW C-C

WIRE LIST						
WIRE NO.	ITEM NO	FROM	TO	COLOR	AWG	LENGTH
1	8	P1-1	SW-1	WHT/VIO	18	7"
2	3	P1-2	SW-2	WHT/BRN	18	7"
3	4	P1-3	SW-3	BLU/BLK	18	7"
4	7	P1-4	SW-4	WHT/ORN	18	7"



DETAIL B
CABLE SCHEMATIC

5. ◁ TERMINATION TRIANGLE INDICATES WIRE NO.

4 TAG HARNESS WITH ASSY NO 0117-0117-10 AND REV LEVEL AS SHOWN

2 IDENTIFY END OF WIRES WITH DESTINATION AS SHOWN

1. DWG IS TO SCALE + MAY BE USED AS A TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

-50	40	30	-20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONS ± 1/64 ANGLES ± 1/2° HOLE SIZE ± 1/64 ANGLES ± 1/2° 0.000 - 0.500 0.000 - 1.000 1.000 - 2.000

DASH NO	NUMBER NEXT ASSEMBLY	QTY
10	0117-0005	1

ENG SERV R. Sycam DATE 2/18/83

DRAWN STM DATE 1-5-83
CHECKED R Wood 2-15-83
PROJECT 2-18-83
MANUFACTURING 2-18-83
QUALITY ASSUR

GOULD biomation

TITLE CABLE ASSEMBLY POWER SWITCH

SCALE | SIZE C | PART NUMBER 0117-0117 | REV A

CODE K105 | SHEET 1 OF 1

0117-0117 | REV A

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	6000-0024-10	CONNECTOR PIN HOUSING	P1	
2									4	6000-0157-10	CONNECTOR PIN		
3									.75	7150-0018-19	WIRE, PVC, 18 AWG, WHT / BRN		
4									.75	7150-0018-37	WIRE, PVC, 18 AWG, BLU / BLK		
5													
6									1	9000-0093-10	POWER SWITCH		
7									.75	7150-0018-20	WIRE, PVC, 18 AWG, WHT / ORG		
8									.75	7150-0018-22	WIRE, PVC, 18 AWG, WHT / VIO		
9									4	6200-0036-10	TERM. FEMALE DISC.		
10									A/R	7200-0008-10	CABLE TIE 4" LNG.		
11									1	7200-0039-10	MARKER. TIE WRAP 4" LNG.		

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL PER ECO 3957	7-16-83	STM	DGW
50	PILOT REL PER ERN 316	1-31-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117 0005	1

		DATE
DWN	STM	8-24-82
CHK	R Wood	2-15-83
ENGR	[signature]	2-18-83
MFG.	[signature]	2-18-83
Q.A.		

LIST OF MATERIAL
CABLE ASSEMBLY-
POWER SWITCH

GOULD biomation

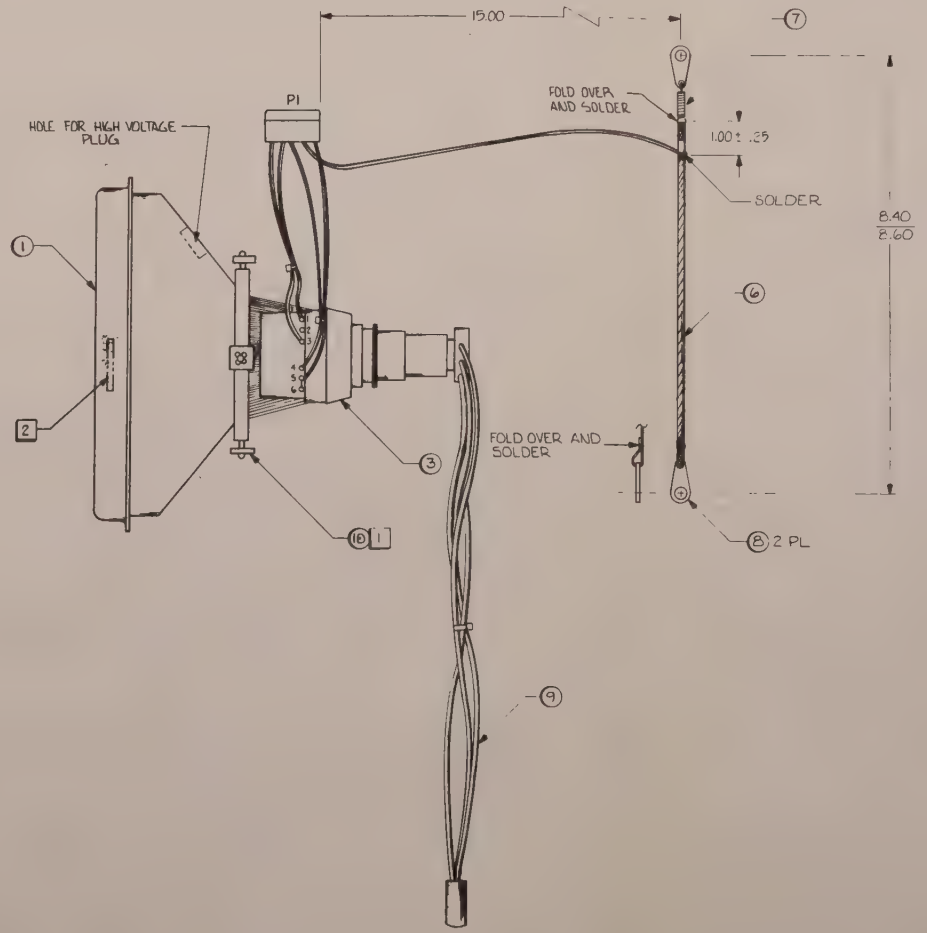
B 0117-0117 REV A

MODEL K105 SHEET 1 OF 1

DWG. NO. 0117-0123 SH 1 REV A

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 309	STM	[illegible]	1/3/83
	51	5773	REVISED PER ECO	MW	[illegible]	[illegible]
	A	5957	PROD. REL PER ECO #	STM	[illegible]	9-6-83



1. MAGNETS ITEM 10 TO BE INSTALLED AT TEST

2. IDENTIFY WITH ASSY NO. 0117-0123 DASH NO. & REV LEVEL WITH 1/8" BLK CHARACTERS

NOTES: UNLESS OTHERWISE SPECIFIED

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONS: .X = ± .1 ANGLES: .XX ± .030 ± 1° .XXX ± .010 HOLE SIZE: 0 .199 ± .004 .000 .000 ± .005 1.000 ± .005 .000

DRAWN STM DATE 9-9-82

CHECKED

PROJ. ENG. [signature] 2/3/83

MANUFACTURING [signature] 2-3-83

QUALITY ASSUR. [signature] 2-3-83

GOULD Instruments Division Santa Clara Operations

TITLE C.R.T. ASSEMBLY

DASH NO	NUMBER	QTY.
10	0117-0003	1
	NEXT ASSEMBLY	

ENG SERV R [signature] DATE 4/3/83

SCALE | SIZE D | PART NUMBER 0117-0123 | REV A

MODEL K105 | SHEET 1 OF 1

ITEM	-90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
	QUANTITY PER ASSEMBLY												
1									1	9000-0029-30	C.R.T.		
2													
3									1	9000-0047-30	DEFLECTION COIL		
4													
5													
6									A/R	7100-0067-10	BRAID	ALPHA 1/16 O.D. APPROX. 7 IN LONG	
7									1	7000-0375-10	SPRING	EXT 1 1/4	
8									2	7090-2006-00	GROUND LUG	#6	
9									1	0117-0021-10	CRT CABLE ASSY		
10									A/R	2000-0006-10	MAGNET		
11													

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD REL PER ECO 3957	9-16-83	STM	DGW
51	REV'D PER ECO 3773	5/24/83	MW	DGW
50	PILOT REL PER ERN 309		STM	GW

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	0117-0003	1

		DATE
DWN	STM	9-9-82
CHK		
ENGR		2/3/83
MFG		2-3-83
Q.A		2-3-83

LIST OF MATERIAL

C.R.T. ASSY

GOULD biomation

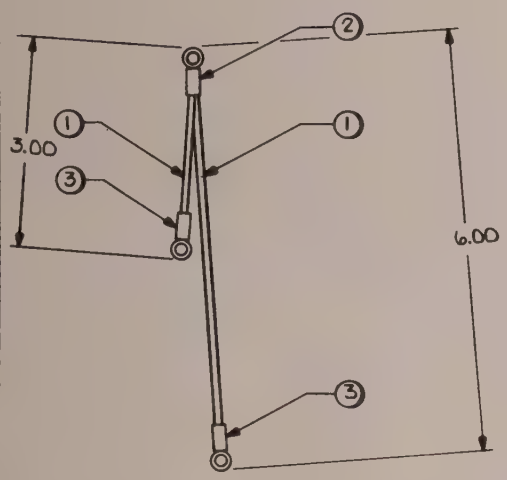
B 0117-0123 REV A

MODEL K105 SHEET 1 OF 1

KLINGLER N-VEL H 10

DWG. NO. 0117-0133 | SH 1 | REV A

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
01		PROTOTYPE	STM		2-4-83
50		PILOT REL. PER ERN 322	[illegible]		2-8-83
51	5872	REVISED PER ECO#	SMC	DGW	7-7-83
A	3957	PROD. REL. PER ECO#	STM	DGW	7-14-83



2. BAG & TAG WITH P/N 0117-0133 DASH NO AND REV LEVEL.
1. DRAWING IS TO SCALE & MAY BE USED AS TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1, .XX ± .020, .XXX ± .010 | ANGLES: ± 1° | HOLE SIZE: 0 to .500 ± .003, .500 to .999 ± .004, 1.000 to 1.499 ± .005

	DRAWN	DATE
	STM	2-4-83
	CHECKED	
	R. Wood	2/28/83
	ENGINEERING	3/1/83
	MANUFACTURING	
	QUALITY ASSUR	3-25-83

DASH NO.	NUMBER	QTY
10	0117-0003	1

ENG SERV: R. Wood DATE 3/25/83

GOULD biomation

TITLE: CHASSIS GND CABLE

SCALE	SIZE	PART NUMBER	REV
1:1	B	0117-0133	A

CODE K105 SHEET 1 OF 1

KLINGLER MVB M

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	LM
1									.75'	7100-0020-10	WIRE STRND 20 GA. BLK		
2									1	6200-0030-10	LUG TERM., TERM RING. TOUNGE BLUE		
3									2	6200-0025-10	LUG TERM., TERM RING. TOUNGE RED		

REV	DESCRIPTION	DATE	DWN	CKD
A	PROD. REL. PER ECO 3957	7-14-83	STM	DGW
51	REVISED PER ECO 5872	7-7-83	SMC	DGW
50	PILOT REL. PER ERN 322	2-8-83	[illegible]	

DASH NO.	NUMBER	QTY
10	0117-0003	1

NEXT ASSEMBLY

		DATE
DWN	STM	2-4-83
CHK	R. Wood	3/25/83
ENGR	[illegible]	3/25/83
MFG.	[illegible]	3-25-83
QA	[illegible]	3-25-83

LIST OF MATERIAL

CHASSIS GND CABLE

GOULD biomation

B 0117-0133 REV A

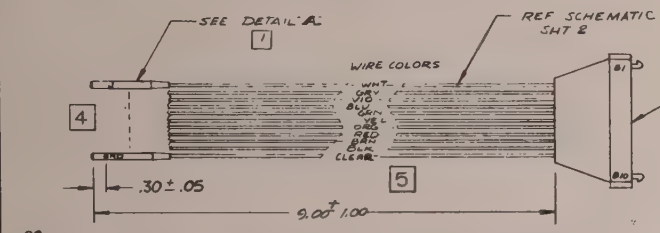
MODEL K105 SHEET 1 OF 1

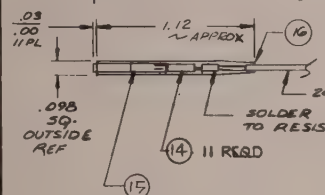
KLINGLER MVB M 10

DWG NO 0117-0294 REV B

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50		PILOT REL PER ECN	SAK		
51	3938	PER ECO	JWC	DJW	7/8/83
A	3957	PROD REL PER ECO N°	JWC	DJW	8/4/83
B	4229	PER ECO 4229	KAREN		1/27/84
B¼	4379	PER ECO 4379	DK		2/27/84

- 10 SHOWN





DETAIL A
SCALE : 2 / 1

NOTES -

1. NOMENCLATURE : CHARACTERS TO BE 8PT, WHITE CAPS. 1 PLACE EACH CONTACT HOUSING (TYPICAL -10,-20,-30 -40 -50 VERSIONS
2. ALL RESISTORS ARE 100Ω ⅛W 5% CARBON COMP.
3. BAG & TAG WITH PART N° 0117-0294, DASH NO AND REV LEVEL.
4. CENTER LEADS IN HOUSING
5. MAX VARIATION OF INDIVIDUAL LEADS (11) SHALL BE .20.

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
50	0120-0057			1				
30	0120-0057			1				
50	0120-0038			2				
30	0120-0038			2				
40	0515-0057			1				
30	0117-3200			4				
ZO								
ID								
DASH NO	NUMBER	QTY	ENG SERV	DATE				

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL: X ± .1, ANGLES ± 1°, XX ± .020, XXX ± .010
HOLE SIZE: 1 - 500 .003; 501 - 999 .004; 1000 UP .005
MACHINING: 1 - 499 .005; 500 UP .010

DRAWN	S. RICO	5/4/83
CHECKED	R. Wood	5/13/83
PROG. ENG.		5/13/83
MANUFACTURING		5/13/83
QUALITY ASSUR.		5/13/83

GOULD biomation

TITLE: ASSY, INPUT CABLE, 11 LEADS, K105

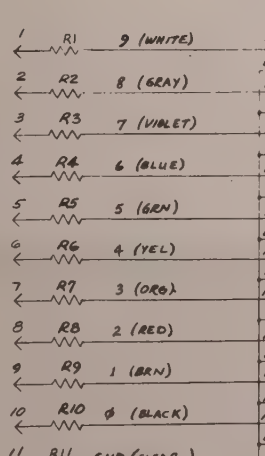
SCALE	SIZE	PART NUMBER	RFV
1/1	B	0117-0294	B

CODE K105 SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO A-4437

DWG NO 0117-0294 REV B

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
		SEE SH 1			



1	DASH				
	-10	-20	-30	-40	-50
	J	R	J	C	R
	–	–	–	–	–
	A	S	K	Q	S
	–	–	–	–	–
	F	7	7	7	F
	–	–	–	–	–
	E	6	6	6	E
	–	–	–	–	–
	D	5	5	5	D
	–	–	–	–	–
	C	4	4	4	C
	–	–	–	–	–
	B	3	3	3	B
	–	–	–	–	–
	A	2	2	2	A
	–	–	–	–	–
	9	1	1	1	9
	–	–	–	–	–
	8	0	0	0	8
	GND	GND	GND	GND	GND

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
DASH NO.	NUMBER	QTY	ENG SERV	DATE				

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS
TOLERANCE

DRAWN	S. RICO	5/4/83
CHECKED	R. Wood	5/13/83
PROG. ENG.		5/13/83
MANUFACTURING		5/13/83
QUALITY ASSUR.		5/13/83

GOULD biomation

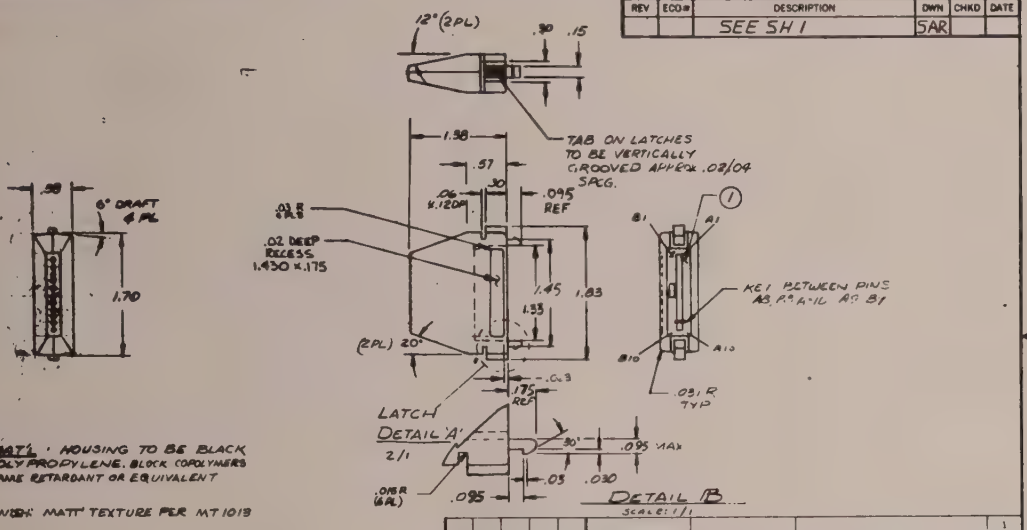
TITLE: ASSY, INPUT CABLE, 11 LEAD, K105

SCALE	SIZE	PART NUMBER	RFV
NONE	B	0117-0294	B

CODE K105 SHEET 2 OF 3

0117-0294 B

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
		SEE SH 1	SAR		



NOTE 1 : HOUSING TO BE BLACK POLYPROPYLENE. BLOCK COPOLYMERS FLAME RETARDANT OR EQUIVALENT

2 FINISH: MATT TEXTURE PER MT 1013

ITEM	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION
1	0117-0294-50	ASSY, INPUT CABLE	11 LEADS, K105
2	0117-0294-40	ASSY, INPUT CABLE	11 LEADS, K105
3	0117-0294-30	ASSY, INPUT CABLE	11 LEADS, K105
4	0117-0294-20	ASSY, INPUT CABLE	11 LEADS, K105
5	0117-0294-10	ASSY, INPUT CABLE	11 LEADS, K105

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE FOR INCHES AND APPLY ONCE PLATED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .025; XXX ± .010

HOLE SIZE: 0 to 500 .005; 500 to 999 .004; 1.000 to 1.999 .005

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	S. RICO	5/4/83
CHECKED	R. Wood	5/13/83
PROJ. ENG.		5/13/83
MANUFACTURING		5/13/83
QUALITY ASSUR		9/14/83
ENG SERV.		DATE

GOULD biomation

TITLE: ASSY, INPUT CABLE 11 LEADS, K105

SCALE	SIZE	PART NUMBER	REV
1/1	B	0117-0294	B

CODE: K105D SHEET 3 OF 3

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1					1	1	1	1	1	6000-0396-30	CONNECTOR, 10 PIN DUAL		
2													
3					A/R	A/R	A/R	A/R	A/R	7100-0121-01	WIRE, WHT, 24 AWG, 105/44		
4					↑	↑	↑	↑	↑	-09	GRY		
5										-10	VIO		
6										-06	BLUE		
7										-04	GRN		
8										-05	YEL		
9										-08	ORG		
10										-03	RED		
11										-07	BRN		
12					↓	↓	↓	↓	↓	-02	BLK		
13					A/R	A/R	A/R	A/R	A/R	7100-0121-11	WIRE, CLEAR, 24 AWG, 105/44		
14					11	11	11	11	11	2950-1000-10	RESISTOR 100Ω, 1/8W, 5%, CAB		
15					11	11	11	11	11	6100-0131-10	SOCKET		
16					11	11	11	11	11	0112-0323-02	CONTACT HSG, BLK NYLON		

REV	DESCRIPTION	DATE	DWN	CKD
A	ORIG REL 3957	7/6/83	DAL	
B	PER ECL 1110	11/1/83	KR	
B1	PER ECO 4379	2-23-84	D.C	

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
-50	0120-1057	1
-50	0120-0036	6
-40	0515-0037	1
-30	0117-3200	4
-30		
-10		

DWN	S. RICO	5/4/83
CHK	R. Wood	5/13/83
ENGR		5/13/83
MFG.		5/13/83
Q.A.		9/21/83

LIST OF MATERIAL

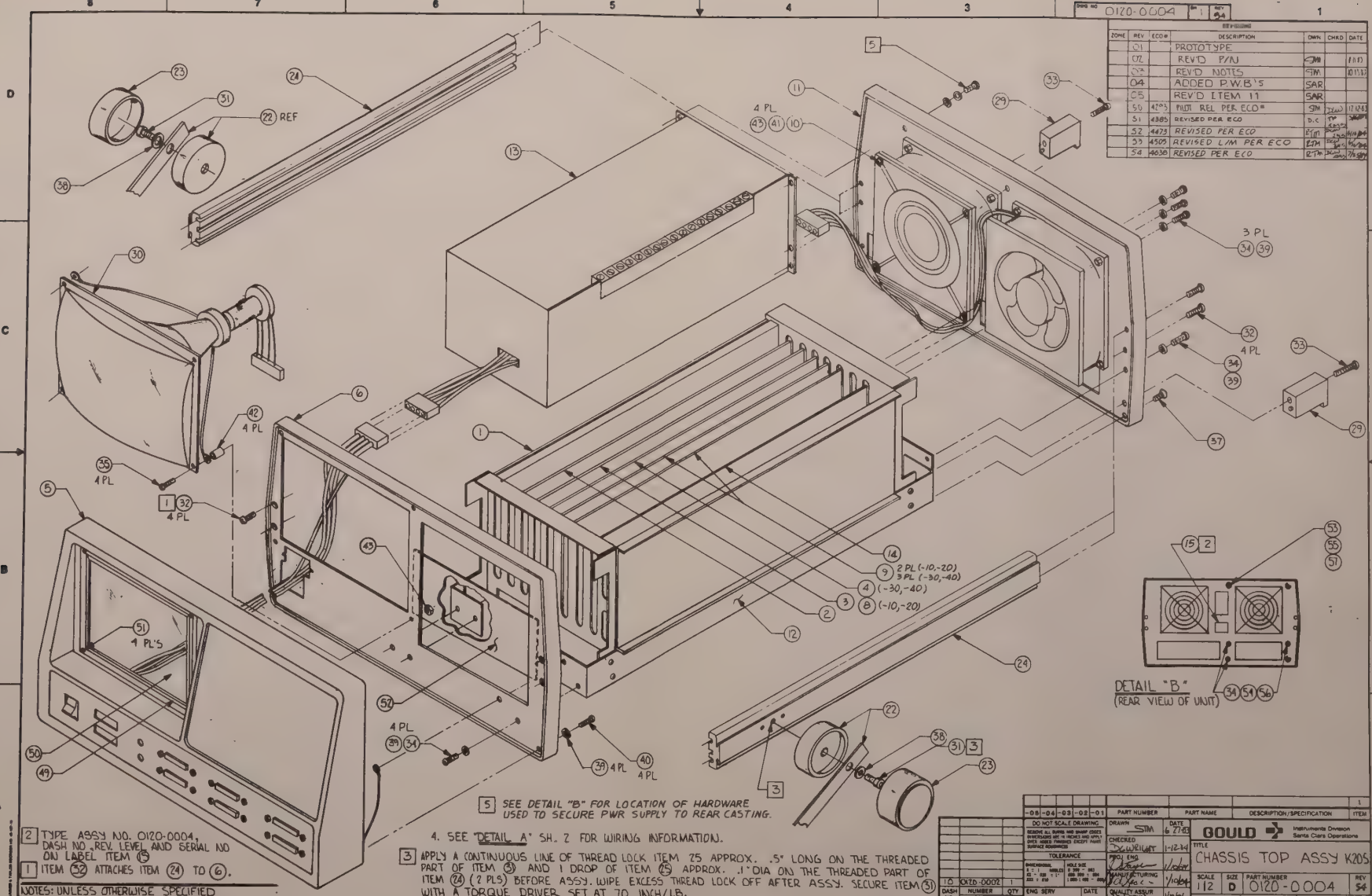
ASSY, INPUT CABLE 11 LEAD, K105

GOULD biomation

B 0117-0294 REV B

MODEL K105 SHEET 1 OF 1

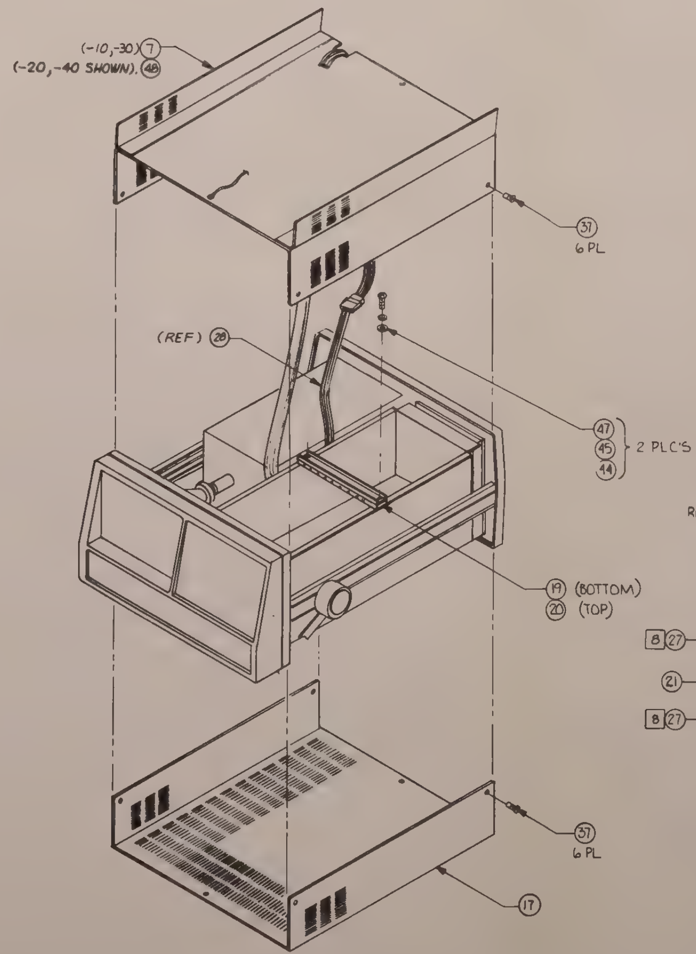
KLINGLER MVIII H10


DWG NO 0120-0004
REV 54
ZONE | REV | ECO # | DESCRIPTION | DWN | CHKD | DATE
01 | PROTOTYPE
02 | REV'D P/N
03 | REV'D NOTES
04 | ADDED P.W.B.'S
05 | REV'D ITEM 11
50 | 4203 | PILOT REL PER ECO*
51 | 4385 | REVISED PER ECO
52 | 4473 | REVISED PER ECO
53 | 4505 | REVISED L/M PER ECO
54 | 4638 | REVISED PER ECO
4 PL
3 PL
2 PL (-10,-20)
3 PL (-30,-40)
(-30,-40)
(-10,-20)
DETAIL "B"
(REAR VIEW OF UNIT)
REF
4 PL'S
2 TYPE ASSY NO. 0120-0004, DASH NO., REV. LEVEL AND SERIAL NO ON LABEL ITEM 15
1 ITEM 32 ATTACHES ITEM 24 TO 6.
NOTES: UNLESS OTHERWISE SPECIFIED
5 SEE DETAIL "B" FOR LOCATION OF HARDWARE USED TO SECURE PWR SUPPLY TO REAR CASTING.
4. SEE "DETAIL A" SH. 2 FOR WIRING INFORMATION.
3 APPLY A CONTINUOUS LINE OF THREAD LOCK ITEM 25 APPROX. .5" LONG ON THE THREADED PART OF ITEM 31 AND 1 DROP OF ITEM 25 APPROX. .1" DIA ON THE THREADED PART OF ITEM 24 (2 PLS) BEFORE ASSY. WIPE EXCESS THREAD LOCK OFF AFTER ASSY. SECURE ITEM 31 WITH A TORQUE DRIVER SET AT 70 INCH/LB.
DO NOT SCALE DRAWING
TOLERANCE
DRAWN STM 6 27 83
CHECKED DG WEIGHT 1-12-84
PROJ ENG 1/10/84
MANUFACTURING 1/10/84
QUALITY ASSUR 1/10/84
PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITEM
GOULD Instruments Division Santa Clara Operations
TITLE CHASSIS TOP ASSY K205
SCALE 1/2 SIZE D PART NUMBER 0120-0004 REV 54
MODEL K205 SHEET 1 OF 2
TO 0120-0002 1
DASH NO | NUMBER | QTY | ENG SERV | DATE
NEXT ASSEMBLY

DWG NO 0120-0004 SH 2 REV 54

REVISIONS

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
			SEE SH. 1			



NOTES: (CONTINUED FROM SHT. 1)

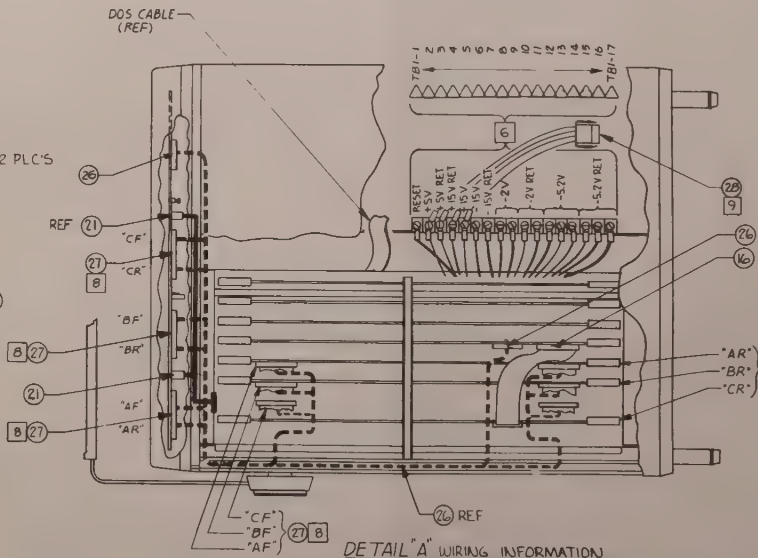
6 NUMBER BESIDE "D" INDICATES WIRE NO. FROM HARNESS 0114-2024-10 WHICH IS SOLDERED INTO CARD CAGE ITEM (12)

7 -10: 32 CH W/O DOS
-20: 32 CH W/DOS
-30: 48 CH W/O DOS
-40 48 CH W/DOS

8 NOTATION TO BE USED ON LABELS FOR CABLE ROUTING.

9 WIRING CHART:

ITEM 28	
PIN NO	TB1-
1	5
2	4
3	3
4	2



DETAIL "A" WIRING INFORMATION

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO	NUMBER	QTY
1D	0120-0002	1
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL X = 1 ANGLES XX = .020 ± 1° XXX = .010
HOLE SIZE

ENG SERV | DATE

DRAWN STM DATE 6-27-83
CHECKED
PROJ ENG
MANUFACTURING 1/10/84
QUALITY ASSUR

GOULD Instruments Division Santa Clara Operations

TITLE CHASSIS TOP ASSY K205

SCALE NONE | SIZE D | PART NUMBER 0120-0004 | REV 54

MODEL K205 | SHEET 2 OF 2

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER ONLY

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1						1	1	1	1	0114-2010-40	ASSY DATA DISPLAY P.W.B.		
2						1	1	1	1	0114-0185-80	ASSY MPU P.W.B.		
3						1	1	1	1	0114-0170-30	ASSY THRESHOLD/G.P.I.B. P.W.B.		
4						1	1	–	–	0114-0160-10	ASSY CLOCK P.W.B. (48 CH)		
5						1	1	1	1	0120-0008-10	FRONT BEZEL ASSY K205		
6						1	1	1	1	0120-0023-10	BEZEL, FRONT, PUNCHED		
7						–	1	–	1	0117-0142-20	COVER, TOP		
8						–	–	1	1	0114-0160-20	ASSY. CLOCK PWB (32 CH)		
9						3	3	2	2	0114-0110-10	ASSY DATA P.W.B.		
10						1	1	1	1	7000-0080-10	FAN GUARD		
11						1	1	1	1	0114-0005-20	REAR CASTING ASSY		
12						1	1	1	1	0120-0022-10	CARD CAGE ASSY		
13						1	1	1	1	9000-0138-10	ASSY. POWER SUPPLY		
14						1	1	1	1	0114-0120-10	ASSY CONTROL P.W.B.		
15						1	1	1	1	6303004O	LABEL, MODEL		
16						1	1	1	1	0114-0054-10	CABLE, CONT. BD. TO CLK. BD.		
17						1	1	1	1	0114-0039-60	COVER, BOTTOM		
18													
19						1	1	1	1	0114-0047-10	CARD RETAINER		
20						1	1	1	1	0114-0049-10	BRACKET, CARD RETAINER		
21						1	1	1	1	0120-0042-01	ASSY, CABLE INPUT TO M.B.	(CLOCK CABLE)	
22						1	1	1	1	0111-0016-10	HANDLE ASSY		
23						2	2	2	2	0111-0059-10	KNOB, BAIL		
24						2	2	2	2	0285-0117-30	EXTRUSION SIDE RAIL		
25						0.01	0.01	0.01	0.01	8200-0032-10	ADHESIVE, THD LOK, #262		
26						1	1	1	1	0120-0043-01	ASSY CABLE PROBE TO CLOCK		
27						3	3	3	3	0120-0044-01	ASSY CABLE INPUT TO DATA		

REV	DESCRIPTION	DATE	DWN	CKD
52	REV'D PER ECO 4473	5-16-84	RTM	DMC
51	REVISED PER ECO 4385	3-1-84	D.C.	MF Jims
50	PILOT REL PER ECO # 4318	11-17-83	STM	DMW
54	REV'D PER ECO 4438	4-25-84	RTM	Mary Jim's DMC
53	REV'D PER ECO 4505	6-8-84	STM	DMC Jim's

DASH NO.	NEXT ASSEMBLY	QTY
10	0120-0002-	1

		DATE
DWN	STM	6-27-83
CHK	D. WRIGHT	7-12-84
ENGR		7/10/84
MFG		7/10/84
Q.A.		7/10/84

LIST OF MATERIAL
CHASSIS TOP ASSEMBLY K205

GOULD ⇒ biomation
B | 0120-0004 | REV 54
MODEL K205 | SHEET 1 OF 2

KLINGLER NAVEL H-10

PLAN HOLD CORPORATION • IRVINE, CALIFORNIA
REORDER BY NUMBER ONLY

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
28						1	1	1	1	0120-0145-10	DOS PWR HARNESS ASSY.		
29						2	2	2	2	0950-0099-10	FOOT REAR		
30						1	1	1	1	0117-0123-10	CRT ASSY		
31						2	2	2	2	7000-0376-10	SCR HD CAP	1/4-20 X 3/4 LG.	
32						8	8	8	8	7000-0328-10	SCR PAN HD	THD ROLLING SCREW #8 X 5/8 LG.	
33						2	2	2	2	7011-1832-60	↕	8-32 X 1 7/8 LG.	
34						11	11	11	11	7011-1632-16	↕	6-32 X 1/2 LG.	
35						4	4	4	4	7011-1632-20	SCR PAN HD	6-32 X 5/8 LG.	
36													
37						13	13	13	13	7021-2632-12	SCR FLAT HD		
38						2	2	2	2	7085-1004-00	WASHER, INT TOOTH STAR	1/4	
39						12	12	12	12	7085-1006-00	WASHER, INT TOOTH STAR	#6	
40						4	4	4	4	7011-1632-12	SCR, PH	6-32 X 3/8 LG.	
41						4	4	4	4	7011-1632-24	SCR PAN HD	6-32 X 3/4 LG.	
42						4	4	4	4	7000-0320-10	SPACER RND	.140 I.D. X .25 O.D. X .125 LG.	
43						5	5	5	5	7070-1632-00	KEPNUT	#6	
44						2	2	2	2	7080-1004-00	WASHER, FLAT	#4 .116 I.D. X .25 O.D. X .032 THK	
45						2	2	2	2	7084-1004-00	WASHER SPLIT-LOCK	#4	
46													
47						2	2	2	2	7011-1440-20	SCR PAN HD CROSS 4-40 X 5/8		
48						1	–	1	–	0114-0468-20	DOS OPTION		
49						1	1	1	1	0120-0019-40	CRT FILTER RETAINER		
50						1	1	1	1	0120-0020-10	CRT FILTER		
51						4	4	4	4	7021-5440-12	SCR. FLT HD PHILIPS	#4 X 3/8 BLK OXIDE	
52						1	1	1	1	0112-0308-10	INSULATOR, KEYBOARD		
53						1	1	1	1	7011-1832-16	SCR PAN HD	#8-32 X 1/2 LG	
54						3	3	3	3	7081-1006-00	WASHER FLAT	#6	
55						1	1	1	1	7081-1008-00	WASHER FLAT	#8	
56						3	3	3	3	7083-1006-00	WASHER SPLIT LOCK	#6	
57						1	1	1	1	7083-1008-00	WASHER SPLIT LOCK	#8	

NOTES
-10: 32 CH W/O DOS
-20: 32 CH W/DOS
-30: 48 CH W/O DOS
-40: 48 CH W/DOS

LIST OF MATERIAL
CHASSIS TOP ASSEMBLY

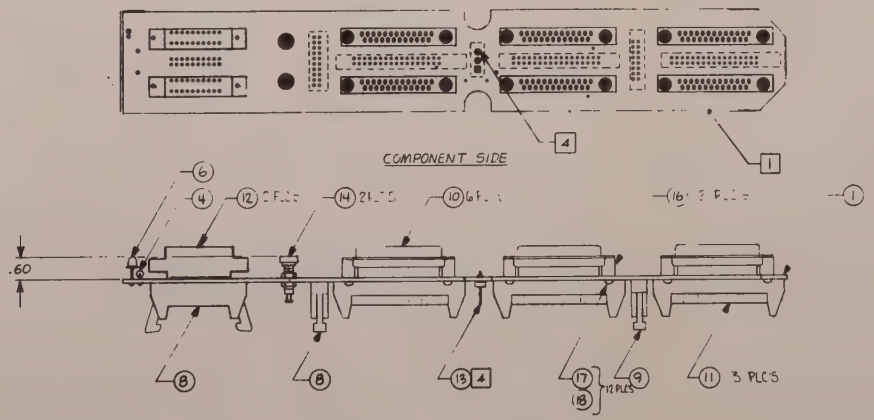
GOULD ⇒ biomation
B | 0120-0004 | REV 54
MODEL K205 | SHEET 2 OF 2

KLINGLER NAVEL H-10

DWG NO	SH	REV
		52

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	02		PROTOTYPE			
			[illegible]			
	50	4343	[illegible]			
			[illegible]			
	52	4638	REVISED PER ECO	KTM		



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSEMBLY DASH NO., REVISION LEVEL AND SERIAL NO. APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. ASSEMBLY REFLECTS SCHEMATIC DRAWING 0120-0026 AND FABRICATION DRAWING 0120-0027
3. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.

4 CUT OFF PIN 3.

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DRAWN D.C DATE 3-22-85

CHECKED

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD Instruments Division Santa Clara Operations

TITLE ASSEMBLY, K205 INPUT BD.

SCALE	SIZE	PART NUMBER	REV
1/1	D	0120-0025	52

MODEL K205 SHEET 1 OF 1

DASH NO	NUMBER	QTY
01	0120-0026	1

NEXT ASSEMBLY

ENG SERV DATE

GOULD

TITLE	LM	DRAWING NO.	REV
ASSEMBLY K205 INPUT BD.		0120-0025	52

DWN	CHK	ENG	MFG	MODEL	SHEET
KAREN				K205	1 OF 2

ITEM NO.	PART NUMBER	QTY PER ASSY -01	-02	-03	-04	-05	U/M	DESCRIPTION	REFERENCE DESIGNATION
1	0120-0027-01	1						FABRICATION, K205 INPUT BD.	
2	0120-0026-01	REF						SCHEMATIC, K205 INPUT BD.	
3									
4	3000-1500-10	1						RESISTOR, 150Ω, 1/4W, 5% C	R1
5									
6	6400-0041-10	1						LED GRN	CR1
7									
8	6000-0271-10	2						CONN, 20 PIN, HDR, ST, DBL, W/E	P5, P6
9	6000-0271-20	1						↑ , 16 PIN, HDR, ST, DBL, W/E	P4
10	6000-0367-10	6						, 25 PIN, D-SUB	J1-J6
11	6000-0585-10	3						, 34 PIN, HDR, ST, DBL, W/E	P1-P3
12	6000-0396-20	2						, 10/20, C-EDG, 4-40 INSR	J7-J8
13	6000-0335-03	1						↓ , 3 PIN, HDR, SGL	P7
14	6000-0041-10	2						CONN, PIN JACK, DVM	J9, J10
15									
16	7000-0426-10	12						STDF, RD, 7/16 LG, 4-40, 3/16 OD.	

REV	ECO	CHK	APPD	DATE
50	4343	DB		1-27-84
51	4442			3/1/84
52	4638	DGW		7/24/84

NOTES:

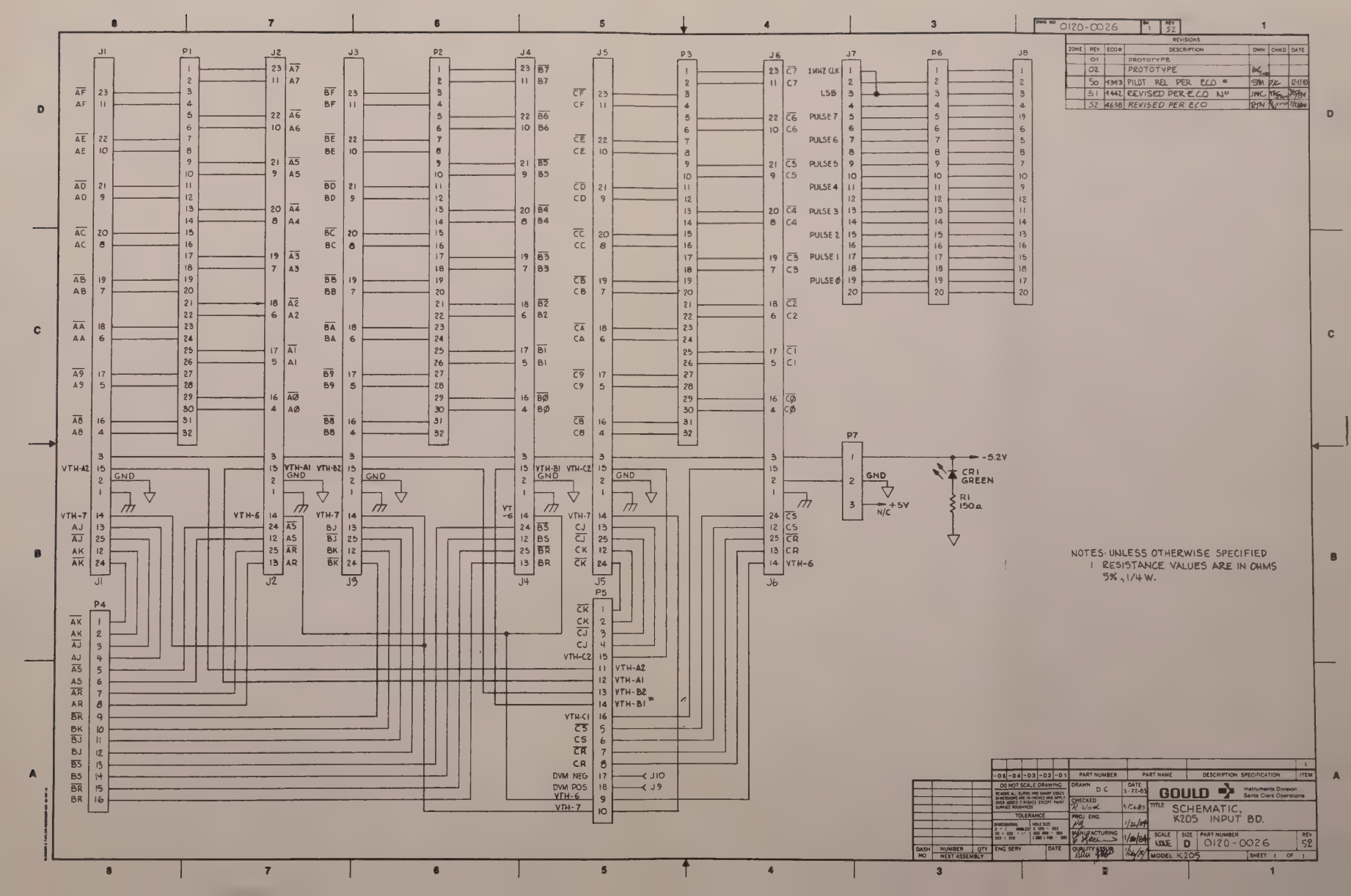
DASH #	NEXT ASSY	QTY
01	0120-0016	1

GOULD

TITLE	LM	DRAWING NO.	REV
ASSEMBLY K205 INPUT BD.		0120-0025	52

MODEL	SHEET
K205	2 OF 2

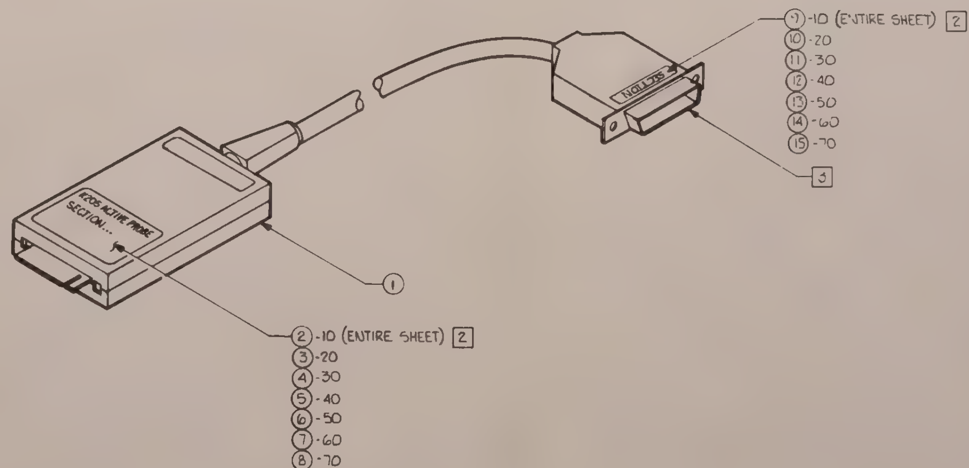
ITEM NO.	PART NUMBER	QTY PER ASSY -01	-02	-03	-04	-05	U/M	DESCRIPTION	REFERENCE DESIGNATION
17	7011-1440-08	12					EA	SCREW, 4/40 X 1/4	
18	7080-1004-00	12					EA	WASHER, FLAT #4 (SMALL PATTERN)	
19									
20									


DWG NO 0120-0026
SH 1
REV 52
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
01 | | PROTOTYPE
02 | | PROTOTYPE
50 | 4343 | PILOT REL PER ECO
51 | 4442 | REVISED PER ECO
52 | 4638 | REVISED PER ECO
J1 J2 J3 J4 J5 J6 J7 J8 P1 P2 P3 P4 P5 P6 P7
1 MHZ CLK
LSB
PULSE 7
PULSE 6
PULSE 5
PULSE 4
PULSE 3
PULSE 2
PULSE 1
PULSE Ø
VTH-A2
VTH-A1
VTH-B2
VTH-B1
VTH-C2
VTH-C1
VTH-6
VTH-7
GND
+5V
N/C
-5.2V
CR1 GREEN
R1 150Ω
DVM NEG
DVM POS
J10
J9
NOTES: UNLESS OTHERWISE SPECIFIED
1 RESISTANCE VALUES ARE IN OHMS 5%, 1/4 W.
PART NUMBER | PART NAME | DESCRIPTION SPECIFICATION | ITEM
DO NOT SCALE DRAWING
DRAWN D C DATE 5-22-03
CHECKED 5/24/03
PROJ. ENG. 1/26/04
MANUFACTURING 1/30/04
QUALITY ASSUR 1/6/04
ENG. SERV DATE
GOULD Instruments Division Santa Clara Operations
TITLE SCHEMATIC, K205 INPUT BD.
SCALE NONE SIZE D PART NUMBER 0120-0026 REV 52
MODEL K205 SHEET 1 OF 1

DWG NO 0120-0031 SH 1 REV 50

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	[illegible]		PROTOTYPE			
	[illegible]		REVISED STRUCTURE	STM		[illegible]
			REVISE CONNECTOR	STM		[illegible]
	50	4293	PILOT REL PER ECO*	STM	[illegible]	12-13-83
	[illegible]	4634	[illegible]	[illegible]	[illegible]	[illegible]



[3] NOTE ORIENTATION OF CONNECTOR SHELL AND LABEL.

[2] ENTIRE SHEET IS USED ONLY WHEN A REPLACEMENT PROBE IS ORDERED.

1. BAG AND TAG WITH PART NO. 0120-0031 DASH NO. AND REV. LEVEL

NOTES: UNLESS OTHERWISE SPECIFIED

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

TOLERANCE

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG SERV | DATE

		DATE
DRAWN	STM	8-24-83
CHECKED	DL WRIGHT	1-12-84
PROJ ENG	[illegible]	[illegible]
MANUFACTURING	[illegible]	[illegible]
QUALITY ASSUR	[illegible]	1/10/84

GOULD Instruments Division Santa Clara Operations

TITLE SPARE PROBE ASSY, K205, 6'

SCALE	SIZE	PART NUMBER	REV
NONE	D	0120-0031	50

MODEL K205 SHEET 1 OF 1

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER 075AR

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER 075AR

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1			1	1	1	1	1	1	1	0117-0099-10	PROBE SUB ASSY		
2									1	0120-0039-10	SECTION LABEL, PROBE POD	(ENTIRE SHEET)	
3								1		0120-0039-20		J.K. 7-0 SECTION A	
4							1			0120-0039-30		R.S. F-8 SECTION A	
5						1				0120-0039-40		J.K. 7-0 SECTION B	
6					1					0120-0039-50		R.S. F-8 SECTION B	
7				1						0120-0039-60		R.S. F-8 SECTION C	
8			1							0120-0039-70	SECTION LABEL, PROBE POD	J.K. 7-0 SECTION C	
9									1	0117-0208-01	SECTION LABEL, OUTPUT CABLE	(ENTIRE SHEET)	
10								1		0117-0208-02		SECTION A 7-0	
11							1			0117-0208-07		SECTION A F-8	
12						1				0117-0208-03		SECTION B 7-0	
13					1					0117-0208-08		SECTION B F-8	
14				1						0117-0208-09		SECTION C F-8	
15			1							0117-0208-04	SECTION LABEL OUTPUT CABLE	SECTION C 7-0	

REV	DESCRIPTION	DATE	DWN	CKD
50BC	PER ECO 4634	7-10-84	[illegible]	DLW JMS
50	PILOT REL PER ECO 4893	12-13-83	STM	DLW
03	REV'D	10-20-83	STM	
02	REVISED STRUCTURE	9-28-83	STM	
01	PROTOTYPE	8-24-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

		DATE
DWN	STM	8-24-83
CHK	D L Wright	7-12-84
ENGR	J Stager	1/10/84
MFG.	[illegible]	1/10/84
Q.A.	Dan Jones	1/10/84

LIST OF MATERIAL

SPARE PROBE ASSY, K205
6'

GOULD biomation

B 0120-0031 REV 50

MODEL K205 SHEET 1 OF 1

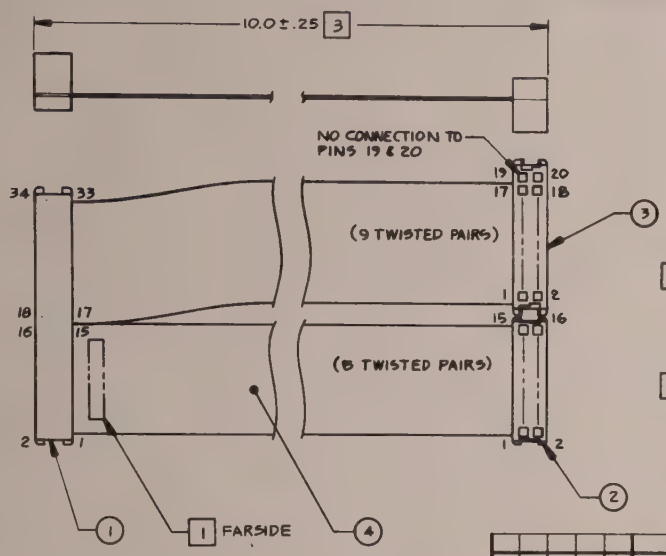
KLINGLER H-VEL H-10

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER 075AR

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER 075AR

DWG. NO. 0120-0042-01 SH 1 REV 51

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4293	PILOT REL. PER ECO	RM	DGW	1/12/84
51	4638	REVISED PER ECO	RTM	DGW JMS	7/23/84



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK CABLE WITH ASSY. NO., DASH NO. & REVISION LEVEL APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK. ALSO STAMP WITH VENDOR I.D.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.
3. CONNECTORS MUST BE INSTALLED ON FLAT PORTIONS OF CABLE.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL .X ± .1 .XX ± .020 .XXX ± .010 ANGLES ± 1° HOLE SIZE 0.599 ± .003 .000 .999 ± .006 1.000 1.499 ± .005

DASH NO	NUMBER	QTY
01	0120-0004	1
	NEXT ASSEMBLY	

ENG. SERV. DATE

		DATE
DRAWN	RMerrer	1/5/84
CHECKED	DGWRIGHT	1-12-84
PROJ. ENG.	[signature]	1/10/84
MANUFACTURING	[signature]	1/10/84
QUALITY ASSUR.	[signature]	1/10/84

GOULD biomation

TITLE ASSEMBLY, CABLE INPUT BD. TO MOTHERBOARD

SCALE	SIZE	PART NUMBER	REV
	B	0120-0042-01	51

CODE K205 SHEET 1 OF 1

KLINGLER [illegible] H

GOULD

TITLE ASSY., CABLE INPUT BD TO MOTHERBOARD

LM

DRAWING NO. 0120-0042-01 REV 51

DWN RM 1/5/84 CHK DGW ENG [signature] MFG [signature]

MODEL K205 SHEET 1 OF 1

ITEM NO.	PART NUMBER	QTY PER ASSY -01	-02	-03	-04	-05	U/M	DESCRIPTION	REFERENCE DESIGNATION
1	6000-0391-20	1						SKT, 34 PIN	
2	6000-0352-20	1						SKT, 16 PIN	
3	6000-0273-10	1						SKT, 20 PIN	
4	7100-0122-10	0.9					FT	CABLE, 34 COND, TWIST AND FLAT	

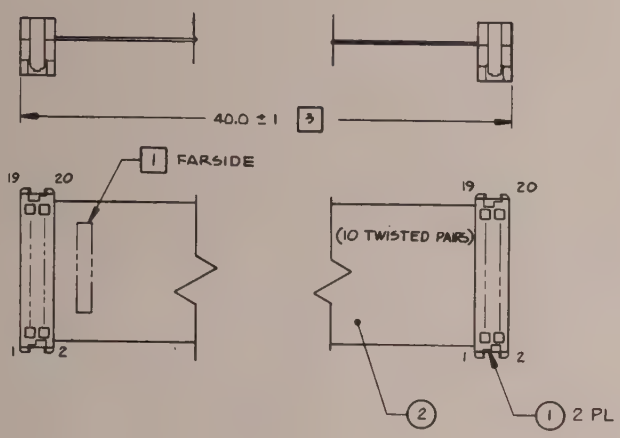
REV	ECO	CHK	APPD	DATE
50	4293	DGW	JMS	1/12/84
51	4638	DGW	JMS	7/24/84

NOTES:

DASH#	NEXT ASSY	QTY
01	0120-0004	1

DWG. NO. 0120-0043-01 SH 1 REV 51

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4293	PILOT REL PER ECO	EM	DGW	1/12/84
51	4468	REVISED PER ECO Nº	JWC	DGW JMC	4/2/84



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK CABLE WITH ASSY. NO., DASH NO. AND REVISION LEVEL APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK. ALSO STAMP WITH VENDOR I.D.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012
3. CONNECTORS MUST BE INSTALLED ON FLAT PORTIONS OF CABLE.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL X ± .1 ANGLES XX ± .020 ± 1° XXX ± .010
HOLE SIZE 0 .599 ± .003 600 .999 ± .004 1 000 1 499 ± .005

DASH NO.	NUMBER	QTY
01	0120-0004	1
	NEXT ASSEMBLY	

ENG SERV. DATE

		DATE
DRAWN	EMERLEY	1/4/83
CHECKED	DGWRIGHT	1-12-84
PROJ. ENG.	[illegible]	1/10/84
MANUFACTURING	[illegible]	1/10/84
QUALITY ASSUR	[illegible]	1/10/84

GOULD biomation

TITLE ASSY., CABLE, PROBE TEST TO CLOCK BD.

SCALE	SIZE	PART NUMBER	REV
NONE	B	0120-0043-01	51

CODE K205 SHEET 1 OF 1

KLINGLER H-VEL H

GOULD

TITLE ASSY, CABLE, PROBE TEST TO CLOCK BD. | LM | DRAWING NO. 0120-0043-01 | REV 51

DWN R.Merley | CHK DGW | ENG [illegible] | MFG [illegible] | MODEL K205 | SHEET 1 OF 1

ITEM NO.	PART NUMBER	QTY PER ASSY -01	-02	-03	-04	-05	U/M	DESCRIPTION	REFERENCE DESIGNATION
1	6000-0273-10	2						SKT, 20 PIN, [illegible]	
2	7100-0068-10	3.3					FT	CABLE, 20 COND, "TWIST AND FLAT"	

REV	ECO	CHK	APPD	DATE
50	4293	DGW		1/12/84
51	4468	DGW	JMS	4/5/84

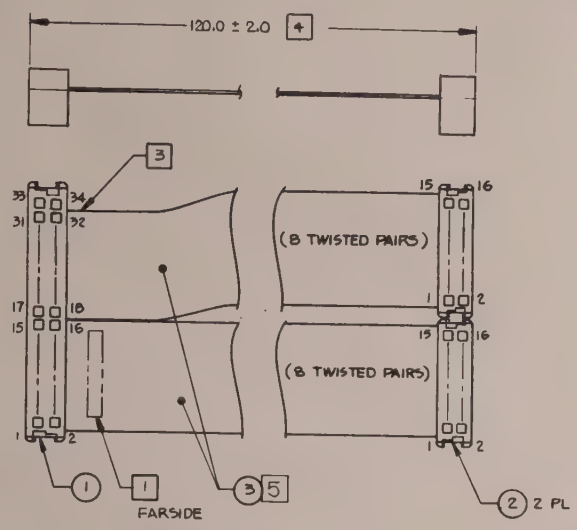
NOTES:

DASH#	NEXT ASSY	QTY
01	0120-0004	1

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER 07SAR

DWG. NO. 0120-0044-01 SH 1 REV 51

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4293	PILOT REL PER ECO	RH	DLW	4/12/84
51	4467	REVISED PER ECO Nº	JWC	DLW JMS	4/12/84



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK CABLE WITH ASSY. NO., DASH NO. AND REVISION LEVEL APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK. ALSO STAMP WITH VENDOR I.D.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.
3. NO CONNECTION TO HEADER ITEM 1 PINS 33 & 34.
4. CONNECTORS MUST BE INSTALLED ON FLAT PORTIONS OF CABLE.
5. CUT CABLE (ITEM 3) INTO TWO TEN FOOT SECTIONS

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°; HOLE SIZE: 0.599 ± .003, .800 .999 ± .004, 1.000 1.499 ± .005

ENG SERV. | DATE

DASH NO	NUMBER	QTY
01	0120-0004	3
	NEXT ASSEMBLY	

		DATE
DRAWN	RHENN	1/5/84
CHECKED	DLW RIGHT	1/12/84
PROJ ENG	[signature]	
MANUFACTURING	[signature]	1/10/84
QUALITY ASSUR	[signature]	1/10/84

GOULD biomation

TITLE ASSEMBLY, CABLE INPUT TO DATA BD.

SCALE	SIZE	PART NUMBER	REV
NONE	B	0120-0044-01	51

CODE K205 SHEET 1 OF 1

KLINGLER H-VEL H

GOULD

TITLE ASSEMBLY, CABLE INPUT TO DATA BD. | LM | DRAWING NO. 0120-0044-01 | REV 51.

DWN RH 1/5/84 | CHK DLW | ENG [signature] | MFG CAC 1/10/84 | MODEL K205 | SHEET 1 OF 1

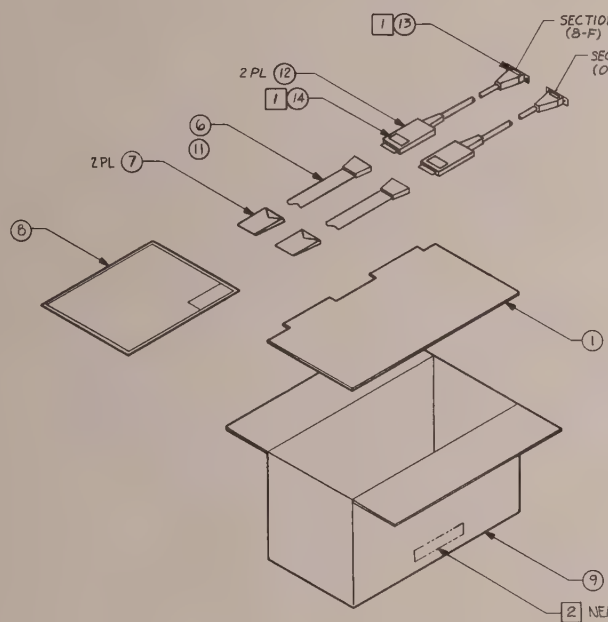
ITEM NO.	PART NUMBER	QTY PER ASSY -01	-02	-03	-04	-05	U/M	DESCRIPTION	REFERENCE DESIGNATION
1	6000-0391-20	1						SKT, 34 PIN	
2	6000-0352-20	2						SKT, 16 PIN	
3	7100-0068-08	20.0					FT	CABLE, 16 COND, "TWIST AND FLAT"	

REV	ECO	CHK	APPD	DATE
50	4293	DLW		1/12/84
51	4467	DLW	JMS	4/12/84

NOTES:

DASH#	NEXT ASSY	QTY
01	0120-0004	3

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE			
	02		REVISED PROBE NO'S	STM		9-26
	03		REV'D P/N ITEM 1	SAR		
	04		REV'D	STM		12-2-83
	50	4293	PILOT REL PER ECO #	STM	DLW	12-13-83
	51	4638	REVISED PER ECO	RTH	DLW	3/24/84



2 IDENTIFY WITH ASSY NO. 0120-0057 DASH NO. AND REV. LEVEL. LOCATE APPROX. AS SHOWN.

1 DISCARD ALL LABELS EXCEPT SECTION C. POD SECTION LABEL (ITEM 14) NOMENCLATURE AND OUTPUT CABLE LABEL (ITEM 13) NOMENCLATURE MUST MATCH.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO	NUMBER NEXT ASSEMBLY	QTY
10	STAND ALONE	N.A.

50	40	30	20	10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE
DIMENSIONAL: ANGLES ± 1° HOLE SIZE: .XX ± .010 .XXX ± .005 .XXX ± .010 .XXXX ± .005 .XXXX ± .005

ENG SERV | DATE

DRAWN STM	DATE 8-24-83	GOULD biomation
CHECKED DLWRIGHT	1/12/84	TITLE K205 SECTION C OPTION
PROJ. ENG J. Stager	1/10/84	
MANUFACTURING E.A. Lecs	1/10/84	SCALE NONE · SIZE C · PART NUMBER 0120-0057 · REV 51
QUALITY ASSUR Nanjing	1/10/84	CODE K205 · SHEET 1 OF 1

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER 075AR

PLAN HOLD CORPORATION • IRVINE CALIFORNIA
REORDER BY NUMBER 075AR

ITEM	QUANTITY PER ASSEMBLY -90	-80	-70	-60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME / DESCRIPTION	REFERENCE DESIGNATION	L/M
1									1	0114-0110-10	ASSY DATA P.W.B.		
2													
3													
4													
5													
6									1	0117-0294-30	INPUT CABLE SET	J.K. 7-0	
7									2	0114-1071-10	GRABBER SET		
8									1	0120-0035-10 ★	INSTRUCTION SHEET C OPT		
9									1	8400-0022-10	SHIPPING BOX		
10													
11									1	0117-0294-50	INPUT CABLE SET	R.S. F-8	
12									2	0117-0099-10	PROBE SUB ASSEMBLY		
13									1	0117-0208-01	SECTION LABEL, OUTPUT		
									1	0120-0039-10	SECTION LABEL, PROBE POD		

★ NOT RELEASED

REV	DESCRIPTION	DATE	DWN	CKD
51	REVISED PER ECO	7-24-84	RTM	DLW
50	PILOT REL PER ECO 4293	12-13-83	STM	DLW
04	DELETED SECTION B PROBE	11-21-83	SAR	
03	REV'D P/N ITEM 1	11-9-83	SAR	
02	REV'D PROBE NO'S	9-28-83	STM	
01	PROTOTYPE	8-24-83	STM	

DASH NO.	NUMBER NEXT ASSEMBLY	QTY
10	STAND ALONE	N.A

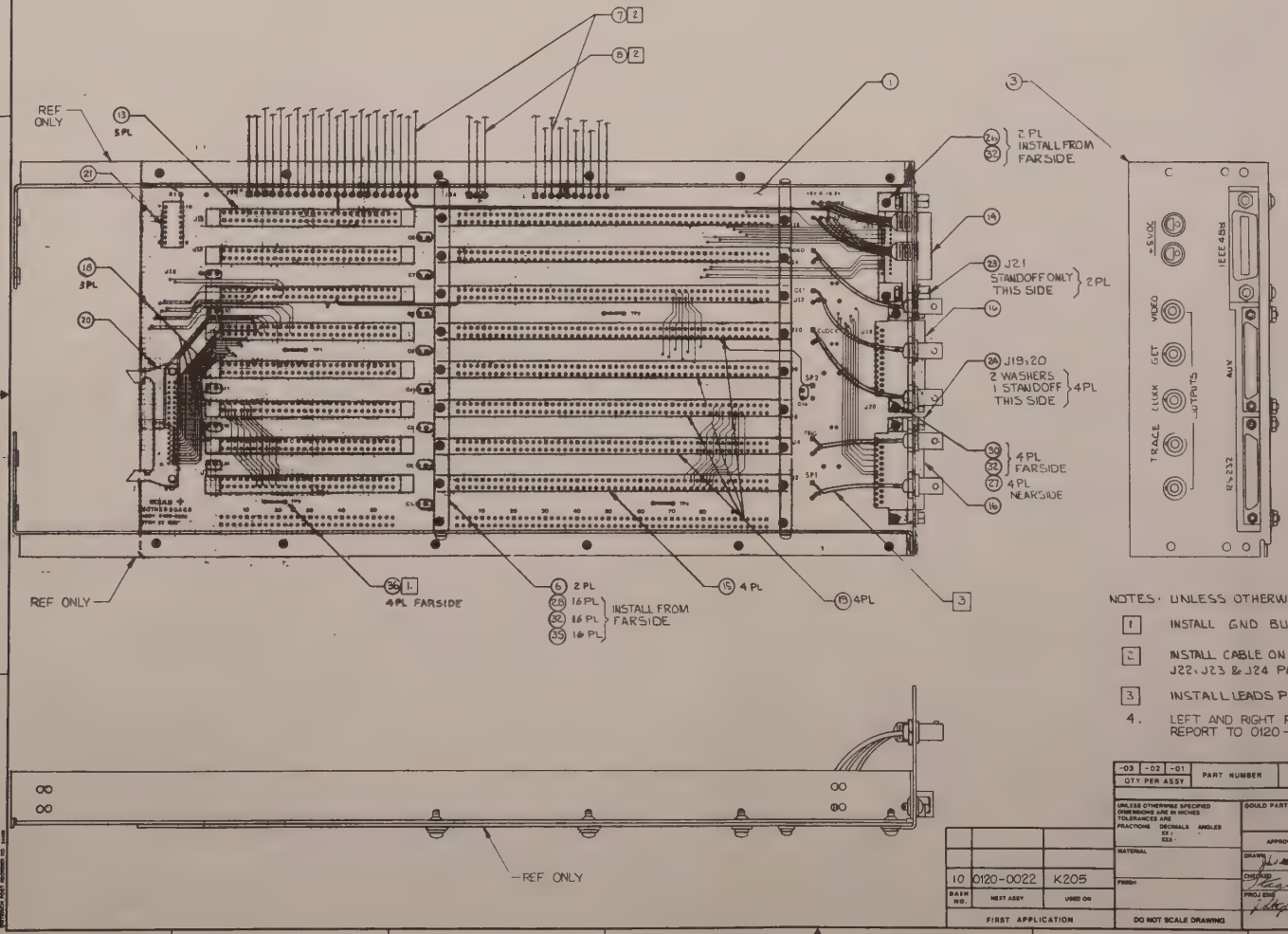
DWN STM	DATE 8-24-83	LIST OF MATERIAL
CHK DLWRIGHT	1/12/84	K205 SECTION C OPTION
ENGR J. Stager	1/10/84	
MFG. E.A. Lecs	1/10/84	
Q.A. Nanjing	1/10/84	

GOULD biomation

B 0120-0057 REV 51

MODEL K205 SHEET 1 OF 1

KLINGLER H-VIL H 10



3 TABLE I

PANEL WIRING			
PANEL		MOTHER BD	
(SPARE)	BNC	SP1	⊡
	SHIELD	SP2	⊙
TRACE	BNC	TRIG	⊡
	SHIELD	TRIG	⊙
CLOCK	BNC	CLOCK	⊡
	SHIELD	CLOCK	⊙
GET	BNC	GET	⊡
	SHIELD	GET	⊙
VIDEO	BNC	VIDEO	⊡
	SHIELD	VIDEO	⊙
LEFT LEMO	GREEN	J25	-5.2V
	BLACK	J25	G
	RED	J25	+5V
RIGHT LEMO	GREEN	J26	-5.2V
	BLACK	J26	G
	RED	J26	+5V

NOTES: UNLESS OTHERWISE SPECIFIED

1. INSTALL GND BUSS WIRE, ITEM 36, ON FARSIDE AT TP1 - 4
2. INSTALL CABLE ON NEARSIDE OF BOARD & SOLDER WIRE TO J22, J23 & J24 PADS.
3. INSTALL LEADS PER TABLE I.
4. LEFT AND RIGHT RAIL SUPPORTS ARE SHOWN FOR CLARITY AND REPORT TO 0120-0022.

DWG NO	SH	REV
0120-0080	1	53

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
53		4537				

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO
QTY PER ASSY					

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
10	0120-0022	K205

FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES XX ± XXX ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN	1-5-84
CHECKED	3/11/84
PROJ ENG	1-17-84

GOULD Electronics

TITLE: ASSEMBLY — MOTHER BOARD PWB K205

SIZE D | DWG NO. 0120-0080 | REV 53

SCALE 1:1 | MODEL K205 | SHEET 1 OF 1

GOULD

TITLE	LM	DRAWING NO.	REV
ASSY – K205 MOTHER PWB	LM	0120-0080	53

DWN	CHK	ENG	MFG	MODEL	SHEET
SAR		Stagert		K205	1 OF 2

ITEM NO.	PART NUMBER	QTY PER ASSY -10	-20	-	-	-	U/M	DESCRIPTION	REFERENCE DESIGNATION
1	0120-0082-10	1						FAB, K205 MOTHER PWB	
2	0120-0081	REF						SCHEM, K205 MOTHER PWB	
3	0120-0092-10	1						ASSY, REAR PANEL M.B.	
4									
5									
6	0114-0038-10	2						SUPPORT BAR	FAB
7	0114-2024-10	1						ASSY, CABLE	FAB
8	0114-0055-20	1						CABLE, ASSEMBLY INPUT BOARD POWER	FAB
9									
10									
11	4000-0025-10	14						CAP, 0.1UF, 20%, 50V, CER	C1-14
12									
13	6000-0198-10	5						CONN, 28 PIN, DUAL	J1,9,11,13,15
14	6000-0315-10	1						CONN, 24 POS, RECEPT	J21 RT ANGL (FOR IEEE 488)
15	6000-0333-10	4						CONN, 50 PIN, DUAL	J2,12,14,16
16	6000-0353-10	2						CONN, 25 POS, RECEPT	J19,J20 RT ANGL (FOR RS232)

REV	ECO	CHK	APPD	DATE
53	4557	DW	JMG	6/23/87

NOTES:

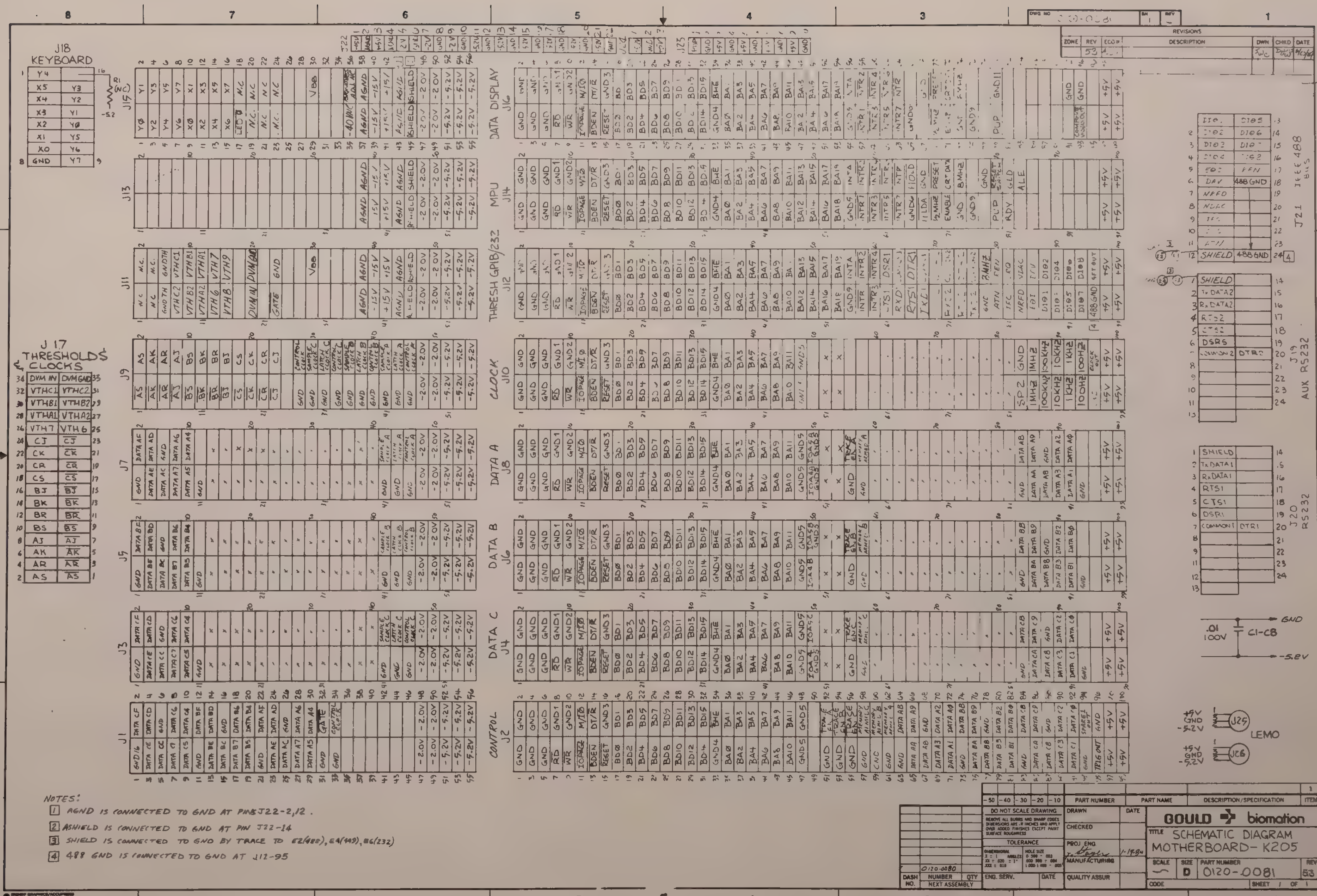
DASH #	NEXT ASSY	QTY
-10	0120-0022	1

GOULD

TITLE	LM	DRAWING NO.	REV
ASSY-K205 MOTHER PWB	LM	0120-0080	53

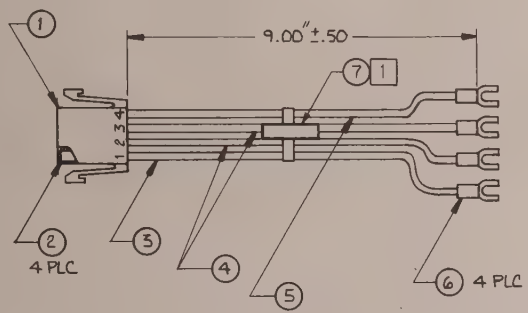
MODEL	SHEET
K205	2 OF 2

ITEM NO.	PART NUMBER	QTY PER ASSY -10	-20	-	-	-	U/M	DESCRIPTION	REFERENCE DESIGNATION
17									
18	6000-0369-10	3						CONN, 28 PIN, DUAL, W/SEL INSR	J3,5,7
19	6000-0370-10	4						CONN, 50 PIN DUAL, W/SEL INSR	J4,6,8,10
20	6000-0373-10	1						CONN, 34 HEADER, RT, ANGLE	J17
21	6100-0120-10	1						SKT, 16 PIN, DIP, LO PROFILE	J18
22									
23	7000-0399-10	1						KIT, MTG. HARDWARE	@ J21
24	7000-0425-10	2						KIT MTG. HARDWARE	@ J19,20
25									
26	7011-1440-10	2						SCR, X, PH, 4-40 x 5/16	
27	7011-1440-12	4						SCR, X, PH, 4-40 x 3/8	
28	7011-1440-16	16						SCR, X, PH, 4-40 X 1/2	
29									
30	7071-1440-00	4						NUT, KEP, #4	
31									
32	7081-1004-00	22						WASHER, FLAT, #4	
33									
34									
35	7085-1004-00	20						WASHER LOCK #4	
36	9000-0054-10	4						BUSS WIRE	TP1-4 (FARSIDE)


J18 KEYBOARD
J17 THRESHOLDS & CLOCKS
DATA DISPLAY J16
MPU J14
THRESH GPIB/232 J12
CLOCK J10
DATA A J8
DATA B J6
DATA C J4
CONTROL J2
J21 IEEE 488 BUS
J19 AUX RS232
J20 RS232
LEMO
NOTES:
1 AGND IS CONNECTED TO GND AT PINS J22-2,12.
2 ASHIELD IS CONNECTED TO GND AT PIN J22-14
3 SHIELD IS CONNECTED TO GND BY TRACE TO E2(488), E4(449), E6(232)
4 488 GND IS CONNECTED TO GND AT J12-95
GOULD biomation
SCHEMATIC DIAGRAM
MOTHERBOARD- K205
D
0120-0081
53
SHEET 1 OF 1

DWG. NO. 0120-0145 SH 1 REV 50

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4604	PROTOTYPE REL	SAR	DGW	7/24/84



1 MARK PART NUMBER, DASH NUMBER REV LEVEL AND VENDOR LOGO (IF APPLICABLE)

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL X = 1 ANGLES .XX = .020 ± 1° .XXX = .010

HOLE SIZE 0.599 ± .003 .600 .999 ± .004 1.000 1.499 ± .008

DASH NO	NUMBER	QTY
-10	0120-0004	1
	NEXT ASSEMBLY	

ENG. SERV. | DATE

DRAWN S. Rico DATE 4-23-84

CHECKED DGW 7/24/84

PROJ. ENG. J. Stayer 7/25/84

MANUFACTURING

QUALITY ASSUR

GOULD

TITLE ASSEMBLY, DOS-PWR HARNESS

SCALE NONE | SIZE B | PART NUMBER 0120-0145 | REV 50

CODE | SHEET 1 OF 1

KLINGLER H-VEL H

GOULD

TITLE ASSEMBLY, DOS-PWR HARNESS

LM

DRAWING NO. 0120-0145

REV 50

DWN S. Rico 4/23/84 | CHK DGW | ENG J. Stayer | MFG | MODEL | SHEET 1 OF 1

ITEM NO.	PART NUMBER	QTY PER ASSY -10	-20	-30	-40	-50	U/M	DESCRIPTION	REFERENCE DESIGNATION
1	6000-0023-10	1					EA	CONN SKT HOUSING	
2	6100-0006-10	4					EA	SKT, 1 PIN, FEMALE	
3	7150-0018-09	.75					FT	WIRE, PVC, 18AWG, WHITE	
4	7150-0018-10	1.5					FT	WIRE, PVC, 18AWG, BLACK	
5	7150-0018-02	.75					FT	WIRE, PVC, 18AWG, RED	
6	6200-0069-10	4					EA	LUG, FORK, 18-22 AWG, RED	
7	7200-0039-10	1					EA	MARKER, TIE WRAP 4" LONG	

REV	ECO	CHK	APPD	DATE
01				
50	4604	DGW	[illegible]	7/24/84

NOTES:

DASH#	NEXT ASSY	QTY
-10	0120-0004	1

GOULD Design & Test Systems Division

The leader in technology, performance and innovation

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Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual: _____ How can this manual be improved: _____

_____

_____

Additional comments: _____

_____

Name _____ Department _____ M/S _____

Company: _____ Manual or Part No. _____

Address _____

City _____ State _____ Zip _____ Phone _____

Warranty/Registration

Please return this card to Gould, Inc. within five days

Did the packaging of this equipment exhibit any outward signs of physical damage ..... YES ○ ○ NO

Did this equipment arrive intact, without missing parts, loose parts or cable damage? ..... YES ○ ○ NO

Did the equipment operate on power-up? ..... YES ○ ○ NO

Did you attain adequate system performance? ..... YES ○ ○ NO

Were any electrical adjustments required? ..... YES ○ ○ NO

If you required assistance, was a local Gould, Inc. representative contacted? ..... YES ○ ○ NO

Comments _____

User Name _____ Title _____ Department _____ M/S _____

Company _____ Phone _____

Address _____ City _____ State _____ Zip _____

Model or Description _____ Serial or Part No. _____ Data Received _____

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